SPEC CPU®2017 Floating Point Speed Result

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Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SS400TR-12L
(3.40 GHz, Intel Xeon E-2224)

$SPECspeed®2017\_fp\_base = 26.3$

$SPECspeed®2017\_fp\_peak = 26.3$

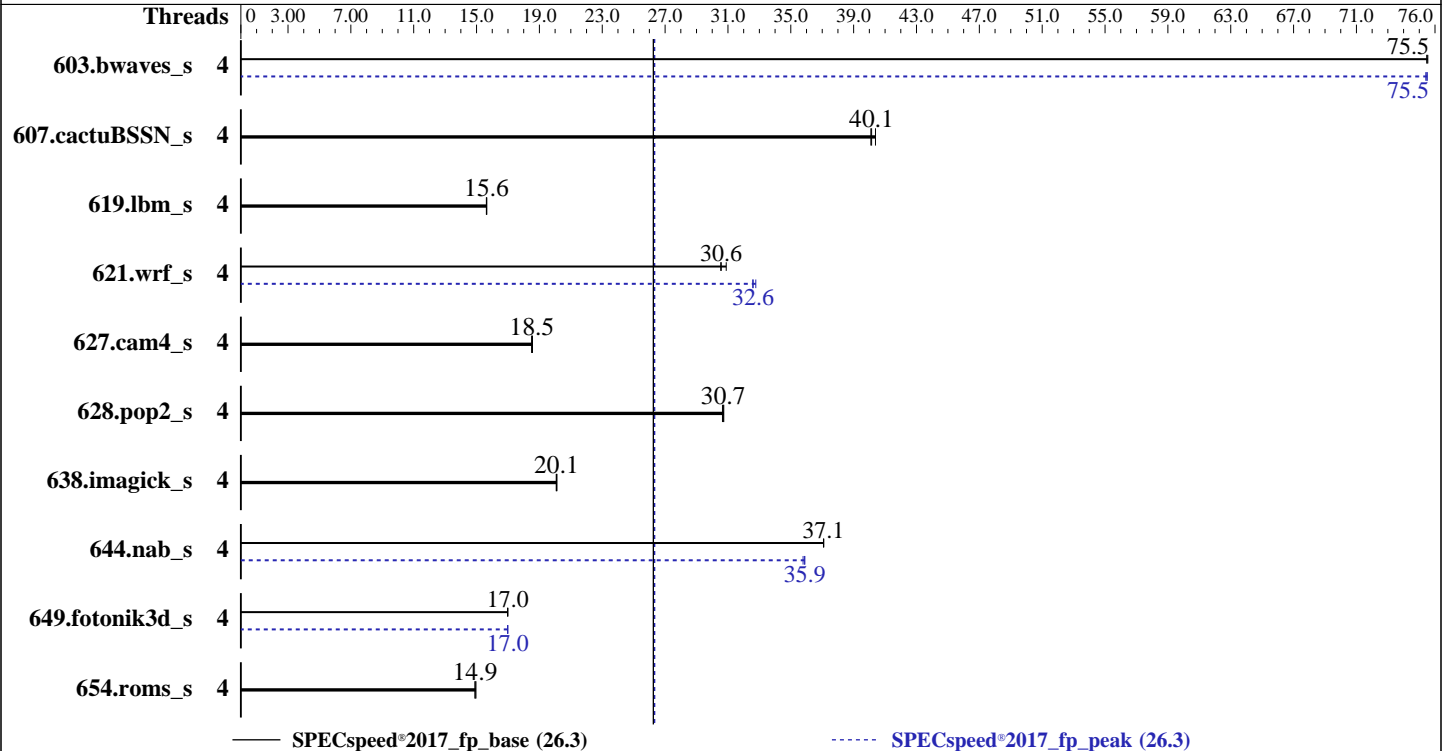|	
CPU2017 License: 006042	**Test Date:** Nov-2021
Test Sponsor: Netweb Pte Ltd	**Hardware Availability:** Apr-2021
Tested by: Tyrone Systems	**Software Availability:** Jun-2021

Threads

Benchmark	Threads	Base	Peak
603.bwaves_s	4	75.5	75.5
607.cactuBSSN_s	4	40.1	
619.lbm_s	4	15.6	
621.wrf_s	4	30.6	32.6
627.cam4_s	4	18.5	
628.pop2_s	4	30.7	
638.imagick_s	4	20.1	
644.nab_s	4	37.1	35.9
649.fotonik3d_s	4	17.0	17.0
654.roms_s	4	14.9	

SPECspeed®2017_fp_base (26.3)   SPECspeed®2017_fp_peak (26.3)

Hardware

CPU Name: Intel Xeon E-2224
 Max MHz: 4600
 Nominal: 3400
 Enabled: 4 cores, 1 chip
 Orderable: 1 Chip
 Cache L1: 32 KB I + 32 KB D on chip per core
  L2: 256 KB I+D on chip per core
  L3: 8 MB I+D on chip per chip
 Other: None
 Memory: 128 GB (4 x 32 GB 2Rx4 PC4-2933P-R, running at 2666)
 Storage: 1 x 480 GB SATA SSD
 Other: None

Software

OS: CentOS Linux release 8.4.2105
  Kernel 4.18.0-305.3.1.el8.x86_64
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++ Compiler Build 20201113 for Linux;
  Fortran: Version 2021.1 of Intel Fortran Compiler Classic Build 20201112 for Linux;
  C/C++: Version 2021.1 of Intel C/C++ Compiler Classic Build 20201112 for Linux
Parallel: Yes
Firmware: Version 1.6 released May-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: Prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base						Peak					
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	4	782	75.5	**782**	**75.5**	781	75.5	4	782	75.4	781	75.5	**782**	**75.5**
607.cactuBSSN_s	4	**415**	**40.1**	416	40.1	413	40.4	4	**415**	**40.1**	416	40.1	413	40.4
619.lbm_s	4	335	15.6	**335**	**15.6**	335	15.6	4	335	15.6	**335**	**15.6**	335	15.6
621.wrf_s	4	**433**	**30.6**	428	30.9	433	30.5	4	404	32.8	406	32.6	**406**	**32.6**
627.cam4_s	4	479	18.5	**478**	**18.5**	478	18.6	4	479	18.5	**478**	**18.5**	478	18.6
628.pop2_s	4	**387**	**30.7**	386	30.7	387	30.7	4	**387**	**30.7**	386	30.7	387	30.7
638.imagick_s	4	719	20.1	717	20.1	**718**	**20.1**	4	719	20.1	717	20.1	**718**	**20.1**
644.nab_s	4	471	37.1	471	37.1	**471**	**37.1**	4	487	35.9	**487**	**35.9**	488	35.8
649.fotonik3d_s	4	537	17.0	**537**	**17.0**	537	17.0	4	**537**	**17.0**	537	17.0	537	17.0
654.roms_s	4	1057	14.9	**1056**	**14.9**	1052	15.0	4	1057	14.9	**1056**	**14.9**	1052	15.0

SPECspeed®2017_fp_base =	**26.3**
SPECspeed®2017_fp_peak =	**26.3**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled locally by Netweb
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the

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Test Sponsor:	Netweb Pte Ltd	**Hardware Availability:**	Apr-2021
Tested by:	Tyrone Systems	**Software Availability:**	Jun-2021

General Notes (Continued)

system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Platform Notes

```
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6622 of 2021-04-07 982a61ec0915b55891ef0e16acafc64d
 running on spec Sun Nov 21 06:31:39 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) E-2224 CPU @ 3.40GHz
       1  "physical id"s (chips)
       4 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 4
       siblings  : 4
       physical 0: cores 0 1 2 3

 From lscpu from util-linux 2.32.1:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
      CPU(s):              4
      On-line CPU(s) list: 0-3
      Thread(s) per core:  1
      Core(s) per socket:  4
      Socket(s):           1
      NUMA node(s):        1
      Vendor ID:           GenuineIntel
      BIOS Vendor ID:      Intel(R) Corporation
      CPU family:          6
      Model:               158
      Model name:          Intel(R) Xeon(R) E-2224 CPU @ 3.40GHz
      BIOS Model name:     Intel(R) Xeon(R) E-2224 CPU @ 3.40GHz
```

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Tested by: Tyrone Systems **Software Availability:** Jun-2021

Platform Notes (Continued)

```
        Stepping:              10
        CPU MHz:               4228.605
        CPU max MHz:           4600.0000
        CPU min MHz:           800.0000
        BogoMIPS:              6816.00
        L1d cache:             32K
        L1i cache:             32K
        L2 cache:              256K
        L3 cache:              8192K
        NUMA node0 CPU(s):     0-3
        Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
    aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer xsave
    avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb invpcid_single pti ssbd
    ibrs ibpb stibp fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm mpx
    rdseed adx smap clflushopt intel_pt xsaveopt xsavec xgetbv1 xsaves dtherm ida arat
    pln pts hwp hwp_notify hwp_act_window hwp_epp md_clear flush_l1d

  /proc/cpuinfo cache data
    cache size : 8192 KB

  From numactl --hardware
  WARNING: a numactl 'node' might or might not correspond to a physical chip.
    available: 1 nodes (0)
    node 0 cpus: 0 1 2 3
    node 0 size: 128821 MB
    node 0 free: 105018 MB
    node distances:
    node   0
      0:  10

  From /proc/meminfo
    MemTotal:       131913240 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

  /sbin/tuned-adm active
     Current active profile: throughput-performance

  /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
    performance

  From /etc/*release* /etc/*version*
    centos-release: CentOS Linux release 8.4.2105
    centos-release-upstream: Derived from Red Hat Enterprise Linux 8.4
```

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Platform Notes (Continued)

```
    os-release:
       NAME="CentOS Linux"
       VERSION="8"
       ID="centos"
       ID_LIKE="rhel fedora"
       VERSION_ID="8"
       PLATFORM_ID="platform:el8"
       PRETTY_NAME="CentOS Linux 8"
       ANSI_COLOR="0;31"
    redhat-release: CentOS Linux release 8.4.2105
    system-release: CentOS Linux release 8.4.2105
    system-release-cpe: cpe:/o:centos:centos:8

  uname -a:
     Linux spec 4.18.0-305.3.1.el8.x86_64 #1 SMP Tue Jun 1 16:14:33 UTC 2021 x86_64 x86_64
     x86_64 GNU/Linux

  Kernel self-reported vulnerability status:

  CVE-2018-12207 (iTLB Multihit):                  KVM: Vulnerable
  CVE-2018-3620 (L1 Terminal Fault):               Mitigation: PTE Inversion
  Microarchitectural Data Sampling:                Mitigation: Clear CPU buffers; SMT
                                                   disabled
  CVE-2017-5754 (Meltdown):                        Mitigation: PTI
  CVE-2018-3639 (Speculative Store Bypass):        Mitigation: Speculative Store
                                                   Bypass disabled via prctl and
                                                   seccomp
  CVE-2017-5753 (Spectre variant 1):               Mitigation: usercopy/swapgs
                                                   barriers and __user pointer
                                                   sanitization
  CVE-2017-5715 (Spectre variant 2):               Mitigation: Full generic
                                                   retpoline, IBPB: conditional,
                                                   IBRS_FW, STIBP: disabled, RSB
                                                   filling
  CVE-2020-0543 (Special Register Buffer Data Sampling): Mitigation: Microcode
  CVE-2019-11135 (TSX Asynchronous Abort):         Mitigation: Clear CPU buffers; SMT
                                                   disabled


  run-level 3 Nov 20 02:58

  SPEC is set to: /home/cpu2017
     Filesystem          Type  Size  Used Avail Use% Mounted on
     /dev/mapper/cl-home xfs   372G  275G   97G  75% /home

  From /sys/devices/virtual/dmi/id
     Vendor:         Tyrone Systems
      Product:        Tyrone Camarero SS400TR-12L
```

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Platform Notes (Continued)

```
     Serial:          0123456789

 Additional information from dmidecode 3.2 follows.  WARNING: Use caution when you
 interpret this section. The 'dmidecode' program reads system data which is "intended to
 allow hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
     4x SK Hynix HMAA4GU7AJR8N-WM 32 GB 2 rank 2933, configured at 2667

 BIOS:
    BIOS Vendor:       American Megatrends Inc.
    BIOS Version:      1.6
    BIOS Date:         05/28/2021
    BIOS Revision:     5.13

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                 | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                  | 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C                 | 644.nab_s(peak)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C                 | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                  | 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
```

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Compiler Version Notes (Continued)

```
C              | 644.nab_s(peak)
-------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------


=========================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
-------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------


=========================================================================
Fortran        | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
               | 654.roms_s(base, peak)
-------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------


=========================================================================
Fortran, C     | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
               | 628.pop2_s(base, peak)
-------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler Classic for applications running on Intel(R)
  64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
-------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icc

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 https://www.spec.org/

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Base Compiler Invocation (Continued)

Fortran benchmarks:
`ifort`

Benchmarks using both Fortran and C:
`ifort icc`

Benchmarks using Fortran, C, and C++:
`icpc icc ifort`

Base Portability Flags

603.bwaves_s: `-DSPEC_LP64`
607.cactuBSSN_s: `-DSPEC_LP64`
619.lbm_s: `-DSPEC_LP64`
621.wrf_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
627.cam4_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
628.pop2_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl`
638.imagick_s: `-DSPEC_LP64`
644.nab_s: `-DSPEC_LP64`
649.fotonik3d_s: `-DSPEC_LP64`
654.roms_s: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries`

Fortran benchmarks:
`-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib -ljemalloc`

Benchmarks using both Fortran and C:
`-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs`

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
```
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Benchmarks using Fortran, C, and C++:
```
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc
```

644.nab_s: `icx`

Fortran benchmarks:
```
ifort
```

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

619.lbm_s: `basepeak = yes`

638.imagick_s: `basepeak = yes`

644.nab_s: `-m64 -Wl,-z,muldefs -xCORE-AVX2 -Ofast -ffast-math`
`-flto -mfpmath=sse -funroll-loops -fiopenmp`
`-DSPEC_OPENMP -qopt-mem-layout-trans=4`

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Peak Optimization Flags (Continued)

644.nab_s (continued):
```
-fimf-accuracy-bits=14:sqrt
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

Fortran benchmarks:

603.bwaves_s: `-m64 -Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2)
```
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: `-m64 -std=c11 -Wl,-z,muldefs -prof-gen`(pass 1)
```
-prof-use(pass 2) -ipo -xCORE-AVX2 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.0-CFL-revA.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.0-CFL-revA.xml

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

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(Test Sponsor: Netweb Pte Ltd)

Tyrone Camarero SS400TR-12L
(3.40 GHz, Intel Xeon E-2224)

SPECspeed®2017_fp_base = 26.3

SPECspeed®2017_fp_peak = 26.3

CPU2017 License: 006042		**Test Date:**	Nov-2021
Test Sponsor:	Netweb Pte Ltd	**Hardware Availability:**	Apr-2021
Tested by:	Tyrone Systems	**Software Availability:**	Jun-2021

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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