SPEC CPU®2017 Floating Point Rate Result

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 383

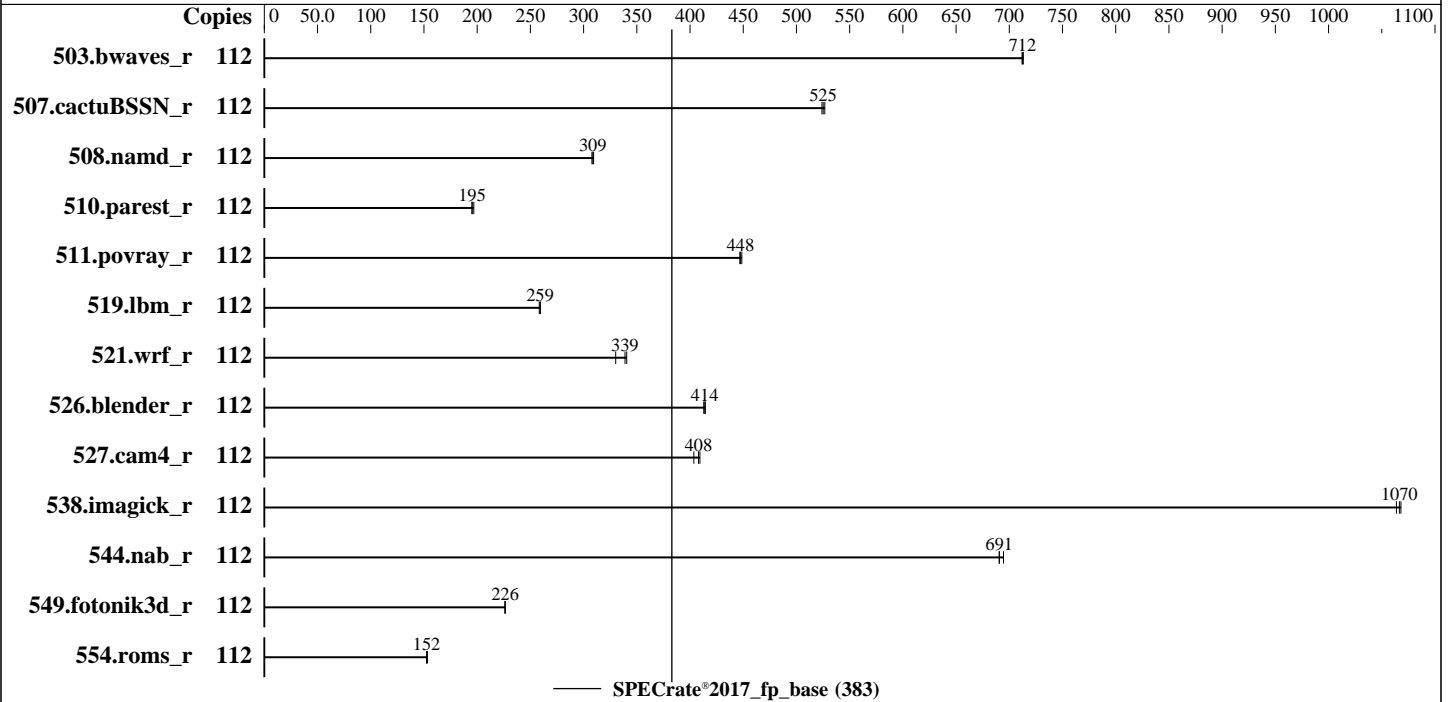SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Benchmark	Copies	Result
503.bwaves_r	112	712
507.cactuBSSN_r	112	525
508.namd_r	112	309
510.parest_r	112	195
511.povray_r	112	448
519.lbm_r	112	259
521.wrf_r	112	339
526.blender_r	112	414
527.cam4_r	112	408
538.imagick_r	112	1070
544.nab_r	112	691
549.fotonik3d_r	112	226
554.roms_r	112	152

SPECrate®2017_fp_base (383)

Hardware

CPU Name: Intel Xeon Gold 6348
 Max MHz: 3500
 Nominal: 2600
Enabled: 56 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 48 KB D on chip per core
 L2: 1.25 MB I+D on chip per core
 L3: 42 MB I+D on chip per chip
 Other: None
Memory: 1 TB (32 x 32 GB 2Rx4 PC4-3200V-R)
Storage: 1 x 300 GB 15K SAS HDD
Other: None

Software

OS: SUSE Linux Enterprise Server 15 SP2
 5.3.18-22-default
Compiler: C/C++: Version 2021.1 of Intel oneAPI DPC++/C++
 Compiler Build 20201113 for Linux;
 Fortran: Version 2021.1 of Intel Fortran Compiler
 Classic Build 20201112 for Linux;
 C/C++: Version 2021.1 of Intel C/C++ Compiler
 Classic Build 20201112 for Linux
Parallel: No
Firmware: Version 4.2.1b released May-2021
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS and OS set to prefer performance at the cost of
 additional power usage

Standard Performance Evaluation Corporation (info@spec.org) https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base =   383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	112	**1576**	**712**	1577	712	1575	713							
507.cactuBSSN_r	112	269	527	**270**	**525**	271	524							
508.namd_r	112	346	308	**345**	**309**	344	309							
510.parest_r	112	1489	197	**1500**	**195**	1502	195							
511.povray_r	112	**584**	**448**	585	447	583	449							
519.lbm_r	112	457	258	**455**	**259**	455	259							
521.wrf_r	112	760	330	737	340	**740**	**339**							
526.blender_r	112	413	413	412	414	**412**	**414**							
527.cam4_r	112	479	409	485	404	**480**	**408**							
538.imagick_r	112	262	1060	**261**	**1070**	261	1070							
544.nab_r	112	**273**	**691**	273	691	271	695							
549.fotonik3d_r	112	1930	226	**1929**	**226**	1928	226							
554.roms_r	112	**1167**	**152**	1161	153	1168	152							

SPECrate®2017_fp_base =   383

SPECrate®2017_fp_peak =   Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7940X CPU + 64GB RAM
memory using openSUSE Leap 15.2
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)   https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 383

SPECrate®2017_fp_peak = Not Run

CPU2017 License:	9019	**Test Date:**	May-2021
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Apr-2021
Tested by:	Cisco Systems	**Software Availability:**	Mar-2021

General Notes (Continued)

```
 sync; echo 3>        /proc/sys/vm/drop_caches
 runcpu command invoked through numactl i.e.:
 numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
 jemalloc, a general purpose malloc implementation
 built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
 running on install Thu May 20 21:56:28 2021

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
       2  "physical id"s (chips)
       112 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 28
       siblings  : 56
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
       25 26 27

 From lscpu:
      Architecture:          x86_64
      CPU op-mode(s):        32-bit, 64-bit
      Byte Order:            Little Endian
      Address sizes:         46 bits physical, 57 bits virtual
```

(Continued on next page)

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2021

Hardware Availability: Apr-2021

Software Availability: Mar-2021

Platform Notes (Continued)

```
        CPU(s):              112
        On-line CPU(s) list: 0-111
        Thread(s) per core:  2
        Core(s) per socket:  28
        Socket(s):           2
        NUMA node(s):        4
        Vendor ID:           GenuineIntel
        CPU family:          6
        Model:               106
        Model name:          Intel(R) Xeon(R) Gold 6348 CPU @ 2.60GHz
        Stepping:            6
        CPU MHz:             800.000
        CPU max MHz:         3500.0000
        CPU min MHz:         800.0000
        BogoMIPS:            5200.00
        Virtualization:      VT-x
        L1d cache:           48K
        L1i cache:           32K
        L2 cache:            1280K
        L3 cache:            43008K
        NUMA node0 CPU(s):   0-13,56-69
        NUMA node1 CPU(s):   14-27,70-83
        NUMA node2 CPU(s):   28-41,84-97
        NUMA node3 CPU(s):   42-55,98-111
        Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
    aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
    xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
    avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 invpcid_single ssbd
    mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid ept_ad
    fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm rdt_a avx512f
    avx512dq rdseed adx smap avx512ifma clflushopt clwb intel_pt avx512cd sha_ni
    avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
    cqm_mbm_local wbnoinvd dtherm ida arat pln pts hwp hwp_act_window hwp_epp
    hwp_pkg_req avx512vbmi umip pku ospke avx512_vbmi2 gfni vaes vpclmulqdq avx512_vnni
    avx512_bitalg tme avx512_vpopcntdq la57 rdpid md_clear pconfig flush_l1d
    arch_capabilities

 /proc/cpuinfo cache data
    cache size : 43008 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 4 nodes (0-3)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 56 57 58 59 60 61 62 63 64 65 66 67 68 69
    node 0 size: 257634 MB
```

(Continued on next page)

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base =   383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

```
   node 0 free: 256827 MB
   node 1 cpus: 14 15 16 17 18 19 20 21 22 23 24 25 26 27 70 71 72 73 74 75 76 77 78 79 80
   81 82 83
   node 1 size: 258041 MB
   node 1 free: 257201 MB
   node 2 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 84 85 86 87 88 89 90 91 92 93 94
   95 96 97
   node 2 size: 258041 MB
   node 2 free: 257447 MB
   node 3 cpus: 42 43 44 45 46 47 48 49 50 51 52 53 54 55 98 99 100 101 102 103 104 105
   106 107 108 109 110 111
   node 3 size: 258004 MB
   node 3 free: 256836 MB
   node distances:
   node   0   1   2   3
     0:  10  11  20  20
     1:  11  10  20  20
     2:  20  20  10  11
     3:  20  20  11  10

 From /proc/meminfo
    MemTotal:       1056482288 kB
    HugePages_Total:        0
    Hugepagesize:       2048 kB

 /sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has
    performance

 From /etc/*release* /etc/*version*
    os-release:
       NAME="SLES"
       VERSION="15-SP2"
       VERSION_ID="15.2"
       PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
       ID="sles"
       ID_LIKE="suse"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:15:sp2"

 uname -a:
    Linux install 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
    x86_64 x86_64 GNU/Linux

 Kernel self-reported vulnerability status:

 CVE-2018-12207 (iTLB Multihit):                        Not affected
 CVE-2018-3620 (L1 Terminal Fault):                     Not affected
```

(Continued on next page)

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

```
Microarchitectural Data Sampling:                      Not affected
CVE-2017-5754 (Meltdown):                              Not affected
CVE-2018-3639 (Speculative Store Bypass):              Mitigation: Speculative Store
                                                       Bypass disabled via prctl and
                                                       seccomp
CVE-2017-5753 (Spectre variant 1):                     Mitigation: usercopy/swapgs
                                                       barriers and __user pointer
                                                       sanitization
CVE-2017-5715 (Spectre variant 2):                     Mitigation: Enhanced IBRS, IBPB:
                                                       conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort):               Not affected


  run-level 3 May 20 14:46


  SPEC is set to: /home/cpu2017
     Filesystem      Type    Size   Used Avail Use% Mounted on
     /dev/sdc2       btrfs   277G   16G   258G   6% /home


  From /sys/devices/virtual/dmi/id
      Vendor:          Cisco Systems Inc
      Product:         UCSC-C240-M6SX
      Serial:          WZP244208SJ


  Additional information from dmidecode follows.  WARNING: Use caution when you interpret
  this section. The 'dmidecode' program reads system data which is "intended to allow
  hardware to be accurately determined", but the intent may not be met, as there are
  frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
      32x 0xCE00 M393A4K40DB3-CWE 32 GB 2 rank 3200


  BIOS:
     BIOS Vendor:       Cisco Systems, Inc.
     BIOS Version:      C240M6.4.2.1b.0.0512210554
     BIOS Date:         05/12/2021
     BIOS Revision:     5.22


  (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C                 | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base = 383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Compiler Version Notes (Continued)

```
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


==============================================================================
C++                | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


==============================================================================
C++, C             | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
--------------------------------------------------------------------------------


==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


==============================================================================
Fortran            | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
--------------------------------------------------------------------------------


==============================================================================
Fortran, C         | 521.wrf_r(base) 527.cam4_r(base)
------------------------------------------------------------------------------
```

(Continued on next page)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base =   383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: May-2021

Hardware Availability: Apr-2021

Software Availability: Mar-2021

Compiler Version Notes (Continued)

```
Intel(R) Fortran Intel(R) 64 Compiler Classic for applications running on
  Intel(R) 64, Version 2021.1 Build 20201112_000000
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) oneAPI DPC++/C++ Compiler for applications running on Intel(R) 64,
  Version 2021.1 Build 20201113
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icx`

C++ benchmarks:
`icpx`

Fortran benchmarks:
`ifort`

Benchmarks using both Fortran and C:
`ifort icx`

Benchmarks using both C and C++:
`icpx icx`

Benchmarks using Fortran, C, and C++:
`icpx icx ifort`

Base Portability Flags

503.bwaves_r: `-DSPEC_LP64`
507.cactuBSSN_r: `-DSPEC_LP64`
508.namd_r: `-DSPEC_LP64`
510.parest_r: `-DSPEC_LP64`
511.povray_r: `-DSPEC_LP64`
519.lbm_r: `-DSPEC_LP64`
521.wrf_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
526.blender_r: `-DSPEC_LP64 -DSPEC_LINUX -funsigned-char`
527.cam4_r: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
538.imagick_r: `-DSPEC_LP64`
544.nab_r: `-DSPEC_LP64`
549.fotonik3d_r: `-DSPEC_LP64`
554.roms_r: `-DSPEC_LP64`

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base =   383

SPECrate®2017_fp_peak = Not Run

CPU2017 License:	9019	**Test Date:**	May-2021
Test Sponsor:	Cisco Systems	**Hardware Availability:**	Apr-2021
Tested by:	Cisco Systems	**Software Availability:**	Mar-2021

Base Optimization Flags

C benchmarks:
```
-w -std=c11 -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

C++ benchmarks:
```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Fortran benchmarks:
```
-w -m64 -Wl,-z,muldefs -xCORE-AVX512 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using both Fortran and C:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using both C and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-mbranches-within-32B-boundaries -ljemalloc
-L/usr/local/jemalloc64-5.0.1/lib
```

Benchmarks using Fortran, C, and C++:
```
-w -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -Ofast -ffast-math
-flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-align array32byte -auto -ljemalloc -L/usr/local/jemalloc64-5.0.1/lib
```

The flags files that were used to format this result can be browsed at
  http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.html
  http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revN.html

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS C240 M6 (Intel Xeon Gold 6348, 2.60GHz)

SPECrate®2017_fp_base =   383

SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: May-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic2021-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revN.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.5 on 2021-05-21 00:56:27-0400.
Report generated on 2021-06-08 20:06:40 by CPU2017 PDF formatter v6442.
Originally published on 2021-06-08.