SPEC CPU®2017 Floating Point Speed Result

Dell Inc.
(Test Sponsor: Dell Inc)

$SPECspeed®2017\_fp\_base = 80.0$

PowerEdge R540 (Intel Xeon Silver 4210R, 2.4 GHz)

$SPECspeed®2017\_fp\_peak = 81.1$

CPU2017 License: 55   **Test Date:** Sep-2020
Test Sponsor: Dell Inc   **Hardware Availability:** Jul-2020
Tested by: Dell Inc.   **Software Availability:** Apr-2020

Threads — scale: 0, 15.0, 30.0, 45.0, 60.0, 75.0, 90.0, 105, 120, 135, 150, 165, 180, 195, 210, 225, 240, 255, 270, 285, 300, 320

Benchmark	Threads	base	peak
603.bwaves_s	20	319	319
607.cactuBSSN_s	20	96.3	
619.lbm_s	20	68.3	
621.wrf_s	20	77.6	82.0
627.cam4_s	20	49.4	
628.pop2_s	20	57.4	
638.imagick_s	20	44.8	
644.nab_s	20	118	124
649.fotonik3d_s	20	63.2	64.7
654.roms_s	20	69.9	

—— SPECspeed®2017_fp_base (80.0)   ----- SPECspeed®2017_fp_peak (81.1)

Hardware

CPU Name: Intel Xeon Silver 4210R
 Max MHz: 3200
 Nominal: 2400
Enabled: 20 cores, 2 chips
Orderable: 1, 2
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 13.75 MB I+D on chip per chip
 Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
Storage: 1 x 480 GB SATA SSD
Other: None

Software

OS: Red Hat Enterprise Linux 8.2
    kernel 4.18.0-193.el8.x86_64
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;
    Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 2.8.1 released Jun-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage

SPEC CPU®2017 Floating Point Speed Result
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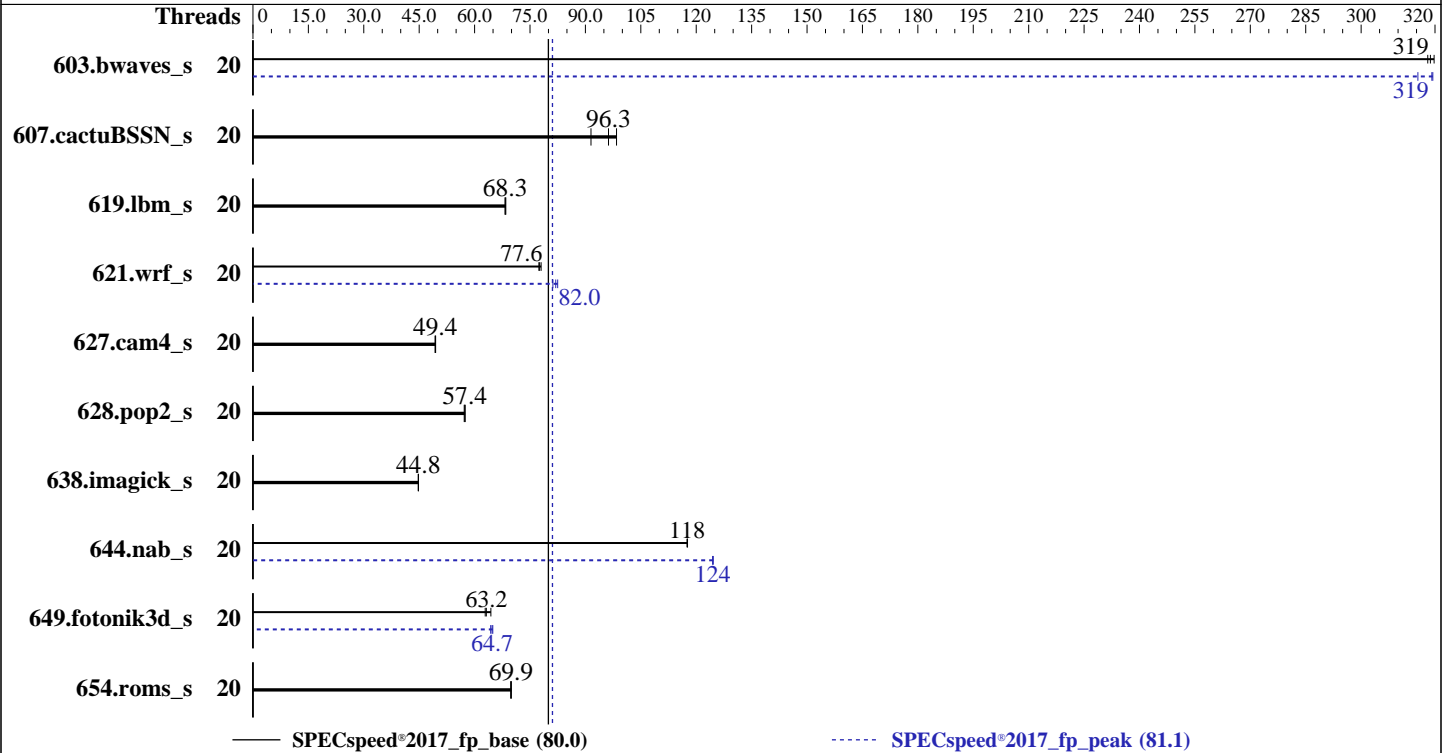
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Results Table

Benchmark	Base						Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	20	**185**	**319**	185	320	186	318	20	185	319	**185**	**319**	187	315
607.cactuBSSN_s	20	169	98.4	182	91.5	**173**	**96.3**	20	169	98.4	182	91.5	**173**	**96.3**
619.lbm_s	20	76.7	68.3	76.5	68.5	**76.7**	**68.3**	20	76.7	68.3	76.5	68.5	**76.7**	**68.3**
621.wrf_s	20	171	77.4	**170**	**77.6**	170	78.0	20	160	82.5	**161**	**82.0**	163	81.2
627.cam4_s	20	179	49.5	**179**	**49.4**	180	49.3	20	179	49.5	**179**	**49.4**	180	49.3
628.pop2_s	20	**207**	**57.4**	208	57.2	207	57.4	20	**207**	**57.4**	208	57.2	207	57.4
638.imagick_s	20	322	44.8	322	44.8	**322**	**44.8**	20	322	44.8	322	44.8	**322**	**44.8**
644.nab_s	20	149	118	149	118	**149**	**118**	20	**140**	**124**	140	124	140	125
649.fotonik3d_s	20	142	64.4	**144**	**63.2**	145	62.9	20	142	64.4	140	64.9	**141**	**64.7**
654.roms_s	20	**225**	**69.9**	226	69.8	225	69.9	20	**225**	**69.9**	226	69.8	225	69.9
SPECspeed®2017_fp_base =		80.0											
SPECspeed®2017_fp_peak =		81.1											

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH =
    "/home/cpu2017-ic19.1u1/lib/intel64:/home/cpu2017-ic19.1u1/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

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Dell Inc.
(Test Sponsor: Dell Inc)

$SPECspeed®2017\_fp\_base = 80.0$

PowerEdge R540 (Intel Xeon Silver 4210R, 2.4 GHz)

$SPECspeed®2017\_fp\_peak = 81.1$

CPU2017 License:	55	**Test Date:**	Sep-2020
Test Sponsor:	Dell Inc	**Hardware Availability:**	Jul-2020
Tested by:	Dell Inc.	**Software Availability:**	Apr-2020

General Notes (Continued)

```
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS settings:
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub set to standard
Logical Processor disabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /home/cpu2017-ic19.1u1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
running on RHEL-8-2-SUT Thu Sep  3 10:39:02 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
      2  "physical id"s (chips)
      20 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following
   excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
      cpu cores : 10
      siblings  : 10
      physical 0: cores 0 1 2 3 4 8 9 10 11 12
      physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
      Architecture:        x86_64
```

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PowerEdge R540 (Intel Xeon Silver 4210R, 2.4 GHz)

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CPU2017 License: 55
Test Sponsor: Dell Inc
Tested by: Dell Inc.

Test Date: Sep-2020
Hardware Availability: Jul-2020
Software Availability: Apr-2020

Platform Notes (Continued)

```
         CPU op-mode(s):        32-bit, 64-bit
         Byte Order:            Little Endian
         CPU(s):                20
         On-line CPU(s) list:   0-19
         Thread(s) per core:    1
         Core(s) per socket:    10
         Socket(s):             2
         NUMA node(s):          2
         Vendor ID:             GenuineIntel
         CPU family:            6
         Model:                 85
         Model name:            Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
         Stepping:              7
         CPU MHz:               1033.170
         CPU max MHz:           3200.0000
         CPU min MHz:           1000.0000
         BogoMIPS:              4800.00
         Virtualization:        VT-x
         L1d cache:             32K
         L1i cache:             32K
         L2 cache:              1024K
         L3 cache:              14080K
         NUMA node0 CPU(s):     0,2,4,6,8,10,12,14,16,18
         NUMA node1 CPU(s):     1,3,5,7,9,11,13,15,17,19
         Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
    aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
    xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
    avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
    invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
    flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
    cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
    avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
    cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
    arch_capabilities

 /proc/cpuinfo cache data
    cache size : 14080 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 2 4 6 8 10 12 14 16 18
    node 0 size: 192075 MB
    node 0 free: 190914 MB
    node 1 cpus: 1 3 5 7 9 11 13 15 17 19
```

(Continued on next page)

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PowerEdge R540 (Intel Xeon Silver 4210R, 2.4 GHz)

$SPECspeed®2017\_fp\_peak = 81.1$

CPU2017 License: 55	**Test Date:** Sep-2020
Test Sponsor: Dell Inc	**Hardware Availability:** Jul-2020
Tested by: Dell Inc.	**Software Availability:** Apr-2020

Platform Notes (Continued)

```
   node 1 size: 193505 MB
   node 1 free: 186379 MB
   node distances:
   node   0   1
     0:  10  21
     1:  21  10

From /proc/meminfo
   MemTotal:       394834884 kB
   HugePages_Total:        0
   Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   os-release:
      NAME="Red Hat Enterprise Linux"
      VERSION="8.2 (Ootpa)"
      ID="rhel"
      ID_LIKE="fedora"
      VERSION_ID="8.2"
      PLATFORM_ID="platform:el8"
      PRETTY_NAME="Red Hat Enterprise Linux 8.2 (Ootpa)"
      ANSI_COLOR="0;31"
   redhat-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
   system-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
   system-release-cpe: cpe:/o:redhat:enterprise_linux:8.2:ga

uname -a:
   Linux RHEL-8-2-SUT 4.18.0-193.el8.x86_64 #1 SMP Fri Mar 27 14:35:58 UTC 2020 x86_64
   x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

itlb_multihit:                         KVM: Vulnerable
CVE-2018-3620 (L1 Terminal Fault):     Not affected
Microarchitectural Data Sampling:      Not affected
CVE-2017-5754 (Meltdown):              Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                        via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):      Mitigation: usercopy/swapgs barriers and __user
                                        pointer sanitization
CVE-2017-5715 (Spectre variant 2):      Mitigation: Enhanced IBRS, IBPB: conditional,
                                        RSB filling
tsx_async_abort:                        Mitigation: Clear CPU buffers; SMT disabled

run-level 3 Sep 3 05:12 last=5

SPEC is set to: /home/cpu2017-ic19.1u1
```

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Platform Notes (Continued)

```
    Filesystem              Type  Size  Used Avail Use% Mounted on
    /dev/mapper/rhel-home xfs   392G   13G  379G   4% /home


 From /sys/devices/virtual/dmi/id
    BIOS:    Dell Inc. 2.8.1 06/30/2020
    Vendor:  Dell Inc.
    Product: PowerEdge R540
    Product Family: PowerEdge


 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
     1x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
     6x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
     5x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
     4x Not Specified Not Specified


 (End of data from sysinfo program)
Memory running at 2400
```

Compiler Version Notes

```
==============================================================================
C                 | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                  | 644.nab_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

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Tested by:	Dell Inc.	**Software Availability:**	Apr-2020

Compiler Version Notes (Continued)

```
==============================================================================
Fortran          | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                 | 654.roms_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
Fortran, C       | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                 | 628.pop2_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc`

Fortran benchmarks:
`ifort`

Benchmarks using both Fortran and C:
`ifort icc`

Benchmarks using Fortran, C, and C++:
`icpc icc ifort`

Base Portability Flags

603.bwaves_s: `-DSPEC_LP64`
607.cactuBSSN_s: `-DSPEC_LP64`
619.lbm_s: `-DSPEC_LP64`
621.wrf_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
627.cam4_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG`

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Base Portability Flags (Continued)

628.pop2_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl`
638.imagick_s: `-DSPEC_LP64`
644.nab_s: `-DSPEC_LP64`
649.fotonik3d_s: `-DSPEC_LP64`
654.roms_s: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries`

Fortran benchmarks:
`-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Benchmarks using both Fortran and C:
`-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Benchmarks using Fortran, C, and C++:
`-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Peak Compiler Invocation

C benchmarks:
`icc`

Fortran benchmarks:
`ifort`

(Continued on next page)

Dell Inc.
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CPU2017 License: 55		**Test Date:**	Sep-2020
Test Sponsor:	Dell Inc	**Hardware Availability:**	Jul-2020
Tested by:	Dell Inc.	**Software Availability:**	Apr-2020

Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
```
ifort icc
```

Benchmarks using Fortran, C, and C++:
```
icpc icc ifort
```

Peak Portability Flags

```
Same as Base Portability Flags
```

Peak Optimization Flags

C benchmarks:

619.lbm_s: basepeak = yes

638.imagick_s: basepeak = yes

644.nab_s: -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

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Peak Optimization Flags (Continued)

621.wrf_s (continued):
```
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.html
http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE12.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE12.xml

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-09-03 11:39:01-0400.
Report generated on 2020-10-14 09:20:44 by CPU2017 PDF formatter v6255.
Originally published on 2020-10-13.