



# SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

New H3C Technologies Co., Ltd.

SPECrate®2017\_int\_base = 115

H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

SPECrate®2017\_int\_peak = Not Run

CPU2017 License: 9066

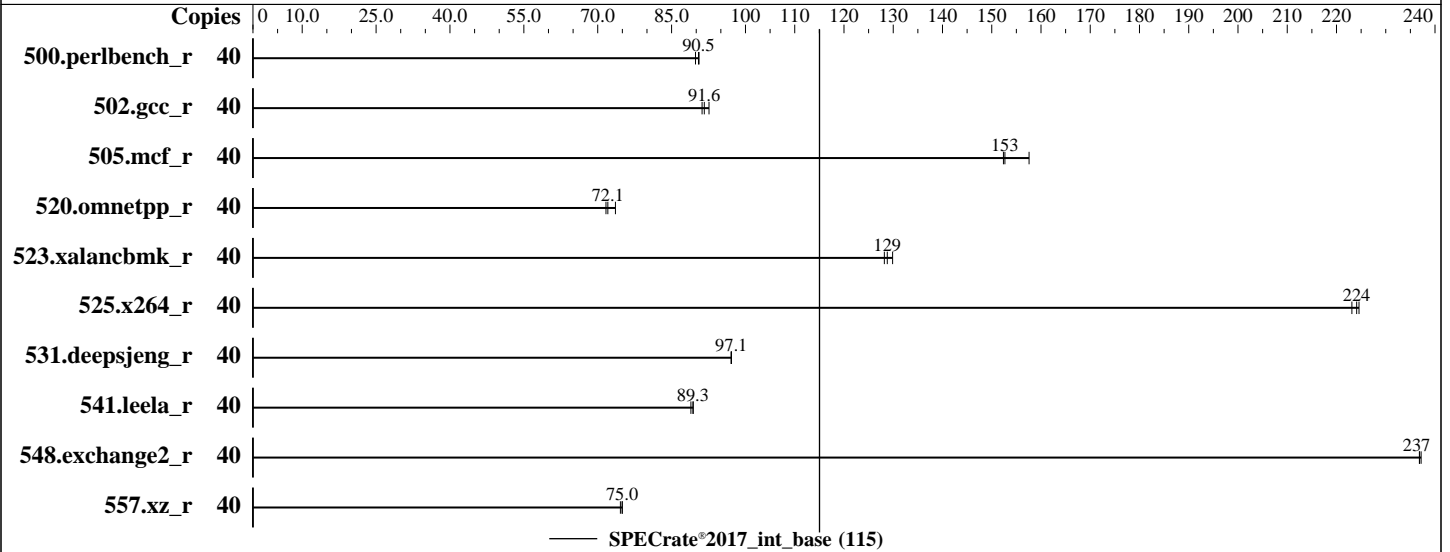
Test Date: Aug-2020

Test Sponsor: New H3C Technologies Co., Ltd.

Hardware Availability: Feb-2020

Tested by: New H3C Technologies Co., Ltd.

Software Availability: May-2019



## Hardware

CPU Name: Intel Xeon Silver 4210R  
 Max MHz: 3200  
 Nominal: 2400  
 Enabled: 20 cores, 2 chips, 2 threads/core  
 Orderable: 1,2 chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 13.75 MB I+D on chip per chip  
 Other: None  
 Memory: 192 GB (12 x 16 GB 2Rx8 PC4-2666V-R, running at 2400)  
 Storage: 1 x 960 GB SATA SSD  
 Other: None

## Software

OS: Red Hat Enterprise Linux Server release 7.6 (Maipo)  
 3.10.0-957.el7.x86\_64  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;  
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux  
 Parallel: No  
 Firmware: Version 2.00.33 released Aug-2019 BIOS  
 File System: xfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: None  
 Power Management: BIOS set to prefer performance at the cost of additional power usage



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## Results Table

Benchmark	Base								Peak							
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio		
500.perlbench_r	40	709	89.9	703	90.6	<b>704</b>	<b>90.5</b>									
502.gcc_r	40	621	91.2	<b>618</b>	<b>91.6</b>	612	92.6									
505.mcf_r	40	410	158	424	152	<b>423</b>	<b>153</b>									
520.omnetpp_r	40	713	73.6	732	71.7	<b>728</b>	<b>72.1</b>									
523.xalancbmk_r	40	325	130	330	128	<b>328</b>	<b>129</b>									
525.x264_r	40	<b>313</b>	<b>224</b>	314	223	312	225									
531.deepsjeng_r	40	472	97.1	<b>472</b>	<b>97.1</b>	472	97.1									
541.leela_r	40	741	89.4	745	88.9	<b>741</b>	<b>89.3</b>									
548.exchange2_r	40	443	237	442	237	<b>442</b>	<b>237</b>									
557.xz_r	40	579	74.6	<b>576</b>	<b>75.0</b>	576	75.0									

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH =
"/home/speccpu/lib/intel64:/home/speccpu/lib/ia32:/home/speccpu/je5.0.1-32"
```

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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## General Notes (Continued)

Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches

## Platform Notes

BIOS Settings:

Set SNC to Enabled  
Set IMC Interleaving to 1-way Interleave  
Set XPT Prefetcher to Enabled

Sysinfo program /home/speccpu/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011  
running on localhost.localdomain Tue Aug 4 22:51:28 2020

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
 2 "physical id"s (chips)
 40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 10
  siblings  : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12
  physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

```
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                40
On-line CPU(s) list:   0-39
Thread(s) per core:    2
Core(s) per socket:    10
Socket(s):              2
NUMA node(s):          2
Vendor ID:              GenuineIntel
CPU family:             6
Model:                  85
Model name:             Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping:               7
```

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## Platform Notes (Continued)

```

CPU MHz:                2877.246
CPU max MHz:            3200.0000
CPU min MHz:            1000.0000
BogoMIPS:                4800.00
Virtualization:         VT-x
L1d cache:              32K
L1i cache:              32K
L2 cache:               1024K
L3 cache:               14080K
NUMA node0 CPU(s):     0-9,20-29
NUMA node1 CPU(s):     10-19,30-39
Flags:                   fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch epb cat_l3 cdp_l3 intel_ppin
intel_pt ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb avx512cd avx512bw avx512vl xsaveopt
xsavec xgetbv1 cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln
pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni spec_ctrl
intel_stibp flush_lld arch_capabilities

```

```

/proc/cpuinfo cache data
cache size : 14080 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
node 0 size: 97878 MB
node 0 free: 88752 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
node 1 size: 98304 MB
node 1 free: 95685 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10

```

```

From /proc/meminfo
MemTotal:      197420128 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

```

From /etc/*release* /etc/*version*

```

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## Platform Notes (Continued)

os-release:

NAME="Red Hat Enterprise Linux Server"

VERSION="7.6 (Maipo)"

ID="rhel"

ID\_LIKE="fedora"

VARIANT="Server"

VARIANT\_ID="server"

VERSION\_ID="7.6"

PRETTY\_NAME="Red Hat Enterprise Linux Server 7.6 (Maipo)"

redhat-release: Red Hat Enterprise Linux Server release 7.6 (Maipo)

system-release: Red Hat Enterprise Linux Server release 7.6 (Maipo)

system-release-cpe: cpe:/o:redhat:enterprise\_linux:7.6:ga:server

uname -a:

Linux localhost.localdomain 3.10.0-957.el7.x86\_64 #1 SMP Thu Oct 4 20:48:51 UTC 2018  
x86\_64 x86\_64 x86\_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected  
Microarchitectural Data Sampling: No status reported  
CVE-2017-5754 (Meltdown): Not affected  
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp  
CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences, \_\_user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS

run-level 3 Aug 4 22:49

SPEC is set to: /home/speccpu

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/mapper/rhel-home	xfs	839G	25G	814G	3%	/home

From /sys/devices/virtual/dmi/id

BIOS: American Megatrends Inc. 2.00.33 08/22/2019

Vendor: New H3C Technologies Co., Ltd.

Product: UniServer R4900 G3

Serial: 210200A00QH18C001552

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

12x Hynix HMA82GR7AFR8N-VK 16 GB 2 rank 2666, configured at 2400

12x NO DIMM NO DIMM

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## Platform Notes (Continued)

(End of data from sysinfo program)

## Compiler Version Notes

```
=====
C          | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base)
          | 525.x264_r(base) 557.xz_r(base)
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
C++       | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
          | 541.leela_r(base)
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran   | 548.exchange2_r(base)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64



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## Base Portability Flags

```
500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalanchmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
```

## Base Optimization Flags

### C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

### C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

### Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>  
[http://www.spec.org/cpu2017/flags/New\\_H3C-Platform-Settings-V1.4-CLX-RevB.html](http://www.spec.org/cpu2017/flags/New_H3C-Platform-Settings-V1.4-CLX-RevB.html)

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>  
[http://www.spec.org/cpu2017/flags/New\\_H3C-Platform-Settings-V1.4-CLX-RevB.xml](http://www.spec.org/cpu2017/flags/New_H3C-Platform-Settings-V1.4-CLX-RevB.xml)



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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

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