



SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Gold 6222V, 1.80GHz)

SPECspeed®2017_int_base = 9.38

SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019

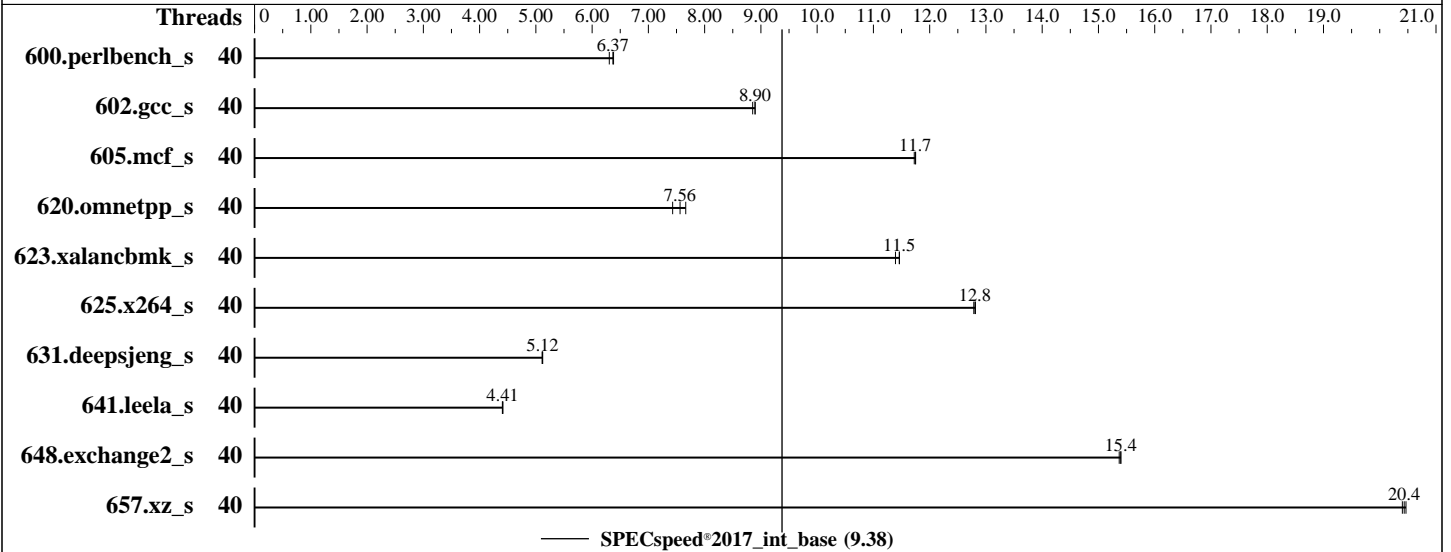
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



Hardware

CPU Name: Intel Xeon Gold 6222V
 Max MHz: 3600
 Nominal: 1800
 Enabled: 40 cores, 2 chips
 Orderable: 1,2 Chips
 Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 27.5 MB I+D on chip per chip
 Other: None
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
 Storage: 1 x 1.9 TB SSD SAS
 Other: None

Software

OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
 Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
 Parallel: Yes
 Firmware: Version 4.0.4b released Apr-2019
 File System: xfs
 System State: Run level 3 (multi-user)
 Base Pointers: 64-bit
 Peak Pointers: Not Applicable
 Other: jemalloc memory allocator V5.0.1
 Power Management: --



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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	40	282	6.31	278	6.38	<u>279</u>	<u>6.37</u>							
602.gcc_s	40	<u>448</u>	<u>8.90</u>	448	8.90	450	8.85							
605.mcf_s	40	402	11.8	<u>402</u>	<u>11.7</u>	403	11.7							
620.omnetpp_s	40	213	7.66	<u>216</u>	<u>7.56</u>	219	7.43							
623.xalancbmk_s	40	<u>124</u>	<u>11.5</u>	124	11.4	124	11.5							
625.x264_s	40	<u>138</u>	<u>12.8</u>	138	12.8	138	12.8							
631.deepsjeng_s	40	280	5.11	<u>280</u>	<u>5.12</u>	280	5.12							
641.leela_s	40	387	4.41	<u>387</u>	<u>4.41</u>	387	4.40							
648.exchange2_s	40	191	15.4	191	15.4	<u>191</u>	<u>15.4</u>							
657.xz_s	40	303	20.4	302	20.5	<u>303</u>	<u>20.4</u>							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



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Platform Notes

BIOS Settings:

```

Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-aixk Fri Sep 6 06:34:00 2019

```

SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo

```

model name      : Intel(R) Xeon(R) Gold 6222V CPU @ 1.80GHz
 2 "physical id"s (chips)
 40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores      : 20
siblings       : 20
physical 0:    cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1:    cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

```

From lscpu:

```

Architecture:    x86_64
CPU op-mode(s):  32-bit, 64-bit
Byte Order:      Little Endian
CPU(s):          40
On-line CPU(s) list: 0-39
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s):       2
NUMA node(s):   2
Vendor ID:       GenuineIntel
CPU family:      6
Model:          85
Model name:      Intel(R) Xeon(R) Gold 6222V CPU @ 1.80GHz
Stepping:       7
CPU MHz:         1800.000
CPU max MHz:     3600.0000
CPU min MHz:     800.0000
BogoMIPS:        3600.00
Virtualization:  VT-x
L1d cache:      32K

```

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Platform Notes (Continued)

```

L1i cache:          32K
L2 cache:           1024K
L3 cache:           28160K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
Flags:              fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmil hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 28160 KB

```

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

```

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 385616 MB
node 0 free: 384751 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
node 1 size: 387015 MB
node 1 free: 386683 MB
node distances:
node 0 1
0: 10 21
1: 21 10

```

```

From /proc/meminfo
MemTotal:          791175672 kB
HugePages_Total:      0
Hugepagesize:       2048 kB

```

```

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"

```

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Platform Notes (Continued)

```
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
Linux linux-aixk 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Sep 5 21:33
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sdb6       xfs   45G   13G   33G   28% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400
```

(End of data from sysinfo program)

Compiler Version Notes

```
=====  
C          | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)  
          | 625.x264_s(base) 657.xz_s(base)  
-----
```

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----
```

```
=====  
C++       | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
         | 641.leela_s(base)  
-----
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----
```

```
=====  
Fortran   | 648.exchange2_s(base)  
-----
```

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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

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Base Optimization Flags (Continued)

C++ benchmarks (continued):

-lqkmalloc

Fortran benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU[®]2017 v1.0.2 on 2019-09-06 09:33:59-0400.

Report generated on 2020-07-13 18:13:36 by CPU2017 PDF formatter v6255.

Originally published on 2019-10-01.