



# SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Bronze 3204, 1.90GHz)

SPECspeed®2017\_int\_base = 4.85

SPECspeed®2017\_int\_peak = Not Run

CPU2017 License: 9019

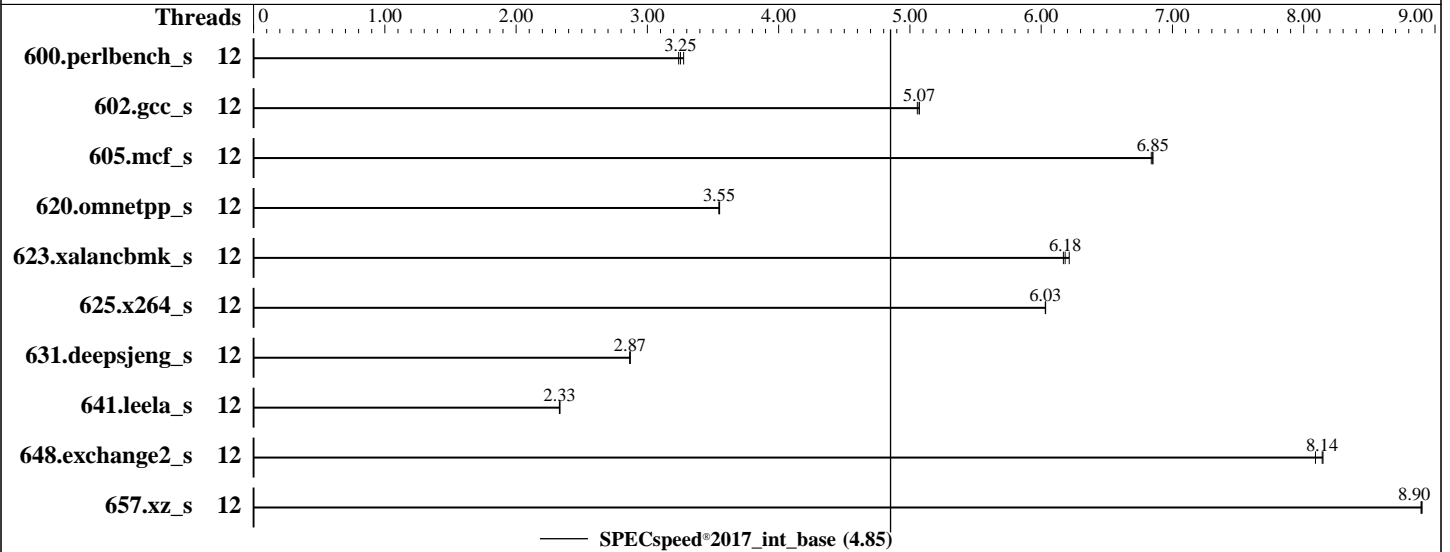
Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Aug-2019

Hardware Availability: Apr-2019

Software Availability: May-2019



### Hardware

CPU Name: Intel Xeon Bronze 3204  
 Max MHz: 1900  
 Nominal: 1900  
 Enabled: 12 cores, 2 chips  
 Orderable: 1,2 chips  
 Cache L1: 32 KB I + 32 KB D on chip per core  
 L2: 1 MB I+D on chip per core  
 L3: 8.25 MB I+D on chip per chip  
 Other: None  
 Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)  
 Storage: 1 x 240 GB M.2 SATA SSD  
 Other: None

### Software

OS: SUSE Linux Enterprise Server 15 (x86\_64) 4.12.14-23-default  
 Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux  
 Parallel: Yes  
 Firmware: Version 4.0.4b released Apr-2019  
 File System: btrfs  
 System State: Run level 3 (multi-user)  
 Base Pointers: 64-bit  
 Peak Pointers: Not Applicable  
 Other: jemalloc memory allocator V5.0.1  
 Power Management: --



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## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	12	542	3.28	548	3.24	<b>546</b>	<b>3.25</b>							
602.gcc_s	12	<b>785</b>	<b>5.07</b>	788	5.06	785	5.07							
605.mcf_s	12	<b>689</b>	<b>6.85</b>	689	6.85	690	6.84							
620.omnetpp_s	12	459	3.55	460	3.55	<b>460</b>	<b>3.55</b>							
623.xalancbmk_s	12	228	6.21	230	6.17	<b>229</b>	<b>6.18</b>							
625.x264_s	12	292	6.03	<b>292</b>	<b>6.03</b>	292	6.03							
631.deepsjeng_s	12	499	2.87	<b>500</b>	<b>2.87</b>	500	2.87							
641.leela_s	12	732	2.33	<b>731</b>	<b>2.33</b>	731	2.33							
648.exchange2_s	12	363	8.09	361	8.15	<b>361</b>	<b>8.14</b>							
657.xz_s	12	694	8.90	<b>695</b>	<b>8.90</b>	695	8.89							

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:  
LD\_LIBRARY\_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation

Filesystem page cache synced and cleared with:  
sync; echo 3> /proc/sys/vm/drop\_caches  
runcpu command invoked through numactl i.e.:  
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)

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## General Notes (Continued)

is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>

## Platform Notes

BIOS Settings:

CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
IMC Interleaving set to Auto  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-5vrl Sat Aug 31 16:31:10 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

From /proc/cpuinfo  
model name : Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz  
2 "physical id"s (chips)  
12 "processors"  
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)  
cpu cores : 6  
siblings : 6  
physical 0: cores 0 1 2 3 4 5  
physical 1: cores 0 1 2 3 4 5

From lscpu:  
Architecture: x86\_64  
CPU op-mode(s): 32-bit, 64-bit  
Byte Order: Little Endian  
CPU(s): 12  
On-line CPU(s) list: 0-11  
Thread(s) per core: 1  
Core(s) per socket: 6  
Socket(s): 2  
NUMA node(s): 2  
Vendor ID: GenuineIntel  
CPU family: 6  
Model: 85

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### Platform Notes (Continued)

```

Model name: Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz
Stepping: 6
CPU MHz: 1900.000
CPU max MHz: 1900.0000
CPU min MHz: 800.0000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 8448K
NUMA node0 CPU(s): 0-5
NUMA node1 CPU(s): 6-11
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke
avx512_vnni arch_capabilities ssbd

```

```

/proc/cpuinfo cache data
cache size : 8448 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5
node 0 size: 385590 MB
node 0 free: 384955 MB
node 1 cpus: 6 7 8 9 10 11
node 1 size: 387047 MB
node 1 free: 382740 MB
node distances:
node  0  1
 0:  10  21
 1:  21  10

```

```

From /proc/meminfo
MemTotal: 791181076 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

```

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## Platform Notes (Continued)

From /etc/\*release\* /etc/\*version\*

os-release:

NAME="SLES"

VERSION="15"

VERSION\_ID="15"

PRETTY\_NAME="SUSE Linux Enterprise Server 15"

ID="sles"

ID\_LIKE="suse"

ANSI\_COLOR="0;32"

CPE\_NAME="cpe:/o:suse:sles:15"

uname -a:

Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86\_64 x86\_64 x86\_64 GNU/Linux

run-level 3 Aug 31 11:44

SPEC is set to: /home/cpu2017

Filesystem	Type	Size	Used	Avail	Use%	Mounted on
/dev/sdb1	btrfs	224G	18G	205G	8%	/home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

Memory:

24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133

(End of data from sysinfo program)

## Compiler Version Notes

```

=====
C      | 600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
      | 625.x264_s(base) 657.xz_s(base)
-----

```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

```

=====
C++   | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
      | 641.leela_s(base)
-----

```

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## Compiler Version Notes (Continued)

```
-----
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

```
=====
Fortran | 648.exchange2_s(base)
-----
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----
```

## Base Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks:

```
icpc -m64
```

Fortran benchmarks:

```
ifort -m64
```

## Base Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```



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## Base Optimization Flags

C benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc
```

C++ benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
```

Fortran benchmarks:

```
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs
```

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.2019-07-31.xml>

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For questions about this result, please contact the tester. For other inquiries, please contact [info@spec.org](mailto:info@spec.org).

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