SPEC® CPU2017 Integer Rate Result

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPECrate2017_int_base = 83.9

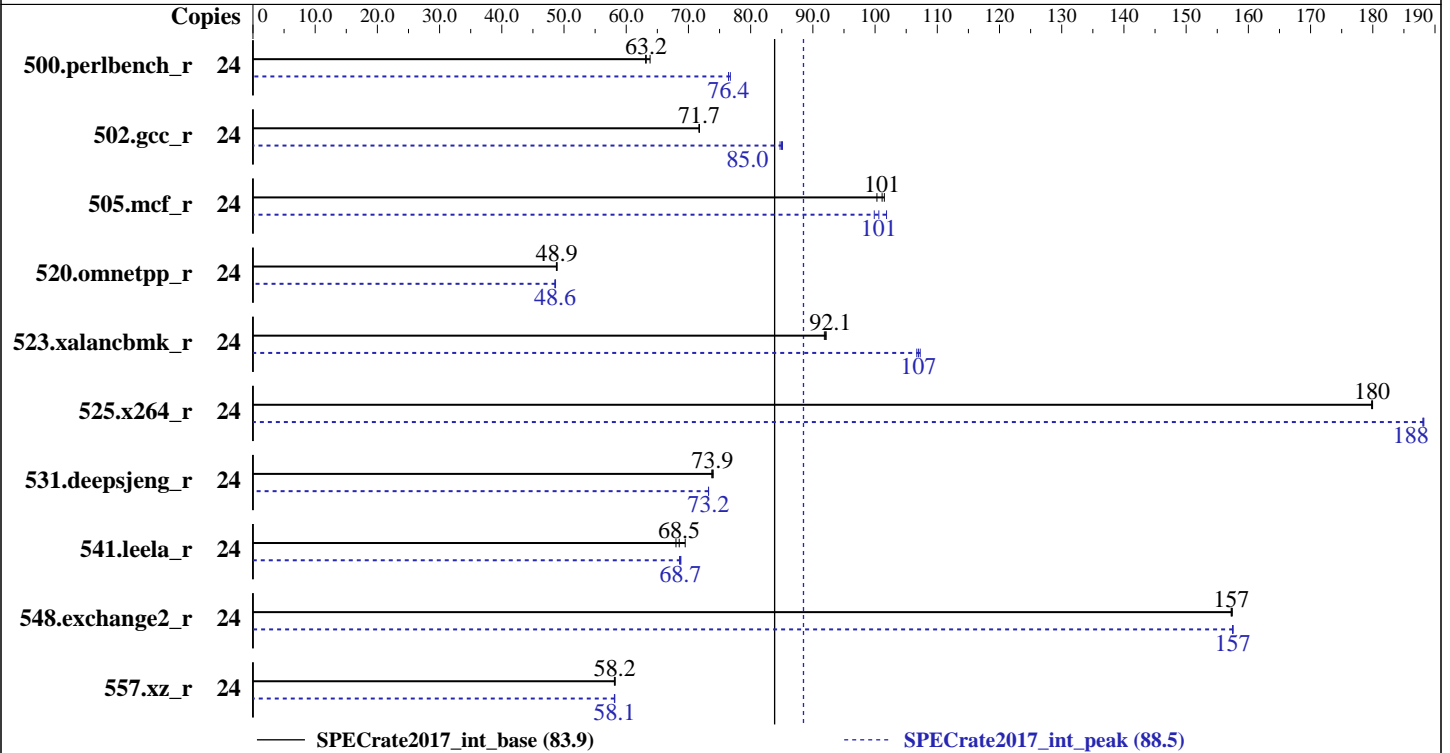SPECrate2017_int_peak = 88.5

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

| Copies | 0 | 10.0 | 20.0 | 30.0 | 40.0 | 50.0 | 60.0 | 70.0 | 80.0 | 90.0 | 100 | 110 | 120 | 130 | 140 | 150 | 160 | 170 | 180 | 190 |

- **500.perlbench_r** 24 — base 63.2, peak 76.4
- **502.gcc_r** 24 — base 71.7, peak 85.0
- **505.mcf_r** 24 — base 101, peak 101
- **520.omnetpp_r** 24 — base 48.9, peak 48.6
- **523.xalancbmk_r** 24 — base 92.1, peak 107
- **525.x264_r** 24 — base 180, peak 188
- **531.deepsjeng_r** 24 — base 73.9, peak 73.2
- **541.leela_r** 24 — base 68.5, peak 68.7
- **548.exchange2_r** 24 — base 157, peak 157
- **557.xz_r** 24 — base 58.2, peak 58.1

—— **SPECrate2017_int_base (83.9)**   ----- **SPECrate2017_int_peak (88.5)**

Hardware

CPU Name: Intel Xeon Gold 6128
 Max MHz.: 3700
 Nominal: 3400
Enabled: 12 cores, 2 chips, 2 threads/core
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
 L2: 1 MB I+D on chip per core
 L3: 19.25 MB I+D on chip per chip
 Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software

OS: SUSE Linux Enterprise Server 12 SP3 (x86_64)
 4.4.120-94.17-default
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
 Compiler for Linux;
 Fortran: Version 19.0.1.144 of Intel Fortran
 Compiler for Linux
Parallel: No
Firmware: Version 4.0.1 released Oct-2018
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 32/64-bit
Other: jemalloc memory allocator V5.0.1

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Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
500.perlbench_r	24	599	63.8	605	63.1	**604**	**63.2**	24	500	76.4	**500**	**76.4**	498	76.7
502.gcc_r	24	**474**	**71.7**	473	71.8	474	71.7	24	399	85.1	401	84.7	**400**	**85.0**
505.mcf_r	24	382	101	387	100	**384**	**101**	24	388	99.9	**386**	**101**	381	102
520.omnetpp_r	24	644	48.9	646	48.8	**645**	**48.9**	24	**648**	**48.6**	649	48.5	647	48.6
523.xalancbmk_r	24	**275**	**92.1**	275	92.1	276	91.8	24	238	107	**237**	**107**	236	107
525.x264_r	24	**234**	**180**	234	180	234	180	24	223	188	223	188	**223**	**188**
531.deepsjeng_r	24	373	73.8	372	74.0	**372**	**73.9**	24	376	73.2	**376**	**73.2**	376	73.2
541.leela_r	24	**580**	**68.5**	572	69.5	585	68.0	24	580	68.6	578	68.8	**578**	**68.7**
548.exchange2_r	24	399	157	**400**	**157**	400	157	24	399	158	399	157	**399**	**157**
557.xz_r	24	446	58.1	445	58.2	**445**	**58.2**	24	**446**	**58.1**	446	58.1	446	58.2
SPECrate2017_int_base =		**83.9**												
SPECrate2017_int_peak =		**88.5**												

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-32:/home/cpu2017/je5.0.1-64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>   /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)

SPEC CPU2017 Integer Rate Result

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Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6128 3.40 GHz)

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General Notes (Continued)

jemalloc: configured and built at default for
32bit (i686) and 64bit (x86_64) targets;
jemalloc: built with the RedHat Enterprise 7.4,
and the system compiler gcc 4.8.5;
jemalloc: sources available from jemalloc.net or
https://github.com/jemalloc/jemalloc/releases

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
 running on linux-4dlf Sat Jan 26 08:53:15 2019

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
       2  "physical id"s (chips)
       24 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 6
       siblings  : 12
       physical 0: cores 0 6 9 10 11 13
       physical 1: cores 0 6 9 10 11 13

 From lscpu:
      Architecture:          x86_64
      CPU op-mode(s):        32-bit, 64-bit
      Byte Order:            Little Endian
      CPU(s):                24
      On-line CPU(s) list:   0-23
      Thread(s) per core:    2
      Core(s) per socket:    6
      Socket(s):             2
      NUMA node(s):          4
      Vendor ID:             GenuineIntel
```

(Continued on next page)

Standard Performance Evaluation Corporation (info@spec.org)

https://www.spec.org/

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPECrate2017_int_base = 83.9

SPECrate2017_int_peak = 88.5

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

Platform Notes (Continued)

```
        CPU family:          6
        Model:               85
        Model name:          Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz
        Stepping:            4
        CPU MHz:             2125.297
        CPU max MHz:         3700.0000
        CPU min MHz:         1200.0000
        BogoMIPS:            6784.05
        Virtualization:      VT-x
        L1d cache:           32K
        L1i cache:           32K
        L2 cache:            1024K
        L3 cache:            19712K
        NUMA node0 CPU(s):   0,2,3,12,14,15
        NUMA node1 CPU(s):   1,4,5,13,16,17
        NUMA node2 CPU(s):   6,8,9,18,20,21
        NUMA node3 CPU(s):   7,10,11,19,22,23
        Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
    aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
    fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
    xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
    dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
    retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
    avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
    clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc pku
    ospke

 /proc/cpuinfo cache data
    cache size : 19712 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 2 3 12 14 15
   node 0 size: 192101 MB
   node 0 free: 190730 MB
   node 1 cpus: 1 4 5 13 16 17
   node 1 size: 193531 MB
   node 1 free: 192235 MB
   node 2 cpus: 6 8 9 18 20 21
   node 2 size: 193531 MB
   node 2 free: 192290 MB
   node 3 cpus: 7 10 11 19 22 23
   node 3 size: 193529 MB
   node 3 free: 192292 MB
```

(Continued on next page)

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPECrate2017_int_base = 83.9

SPECrate2017_int_peak = 88.5

CPU2017 License: 9019

Test Sponsor: Cisco Systems

Tested by: Cisco Systems

Test Date: Jan-2019

Hardware Availability: Aug-2017

Software Availability: Nov-2018

Platform Notes (Continued)

```
   node distances:
   node   0   1   2   3
     0:  10  11  21  21
     1:  11  10  21  21
     2:  21  21  10  11
     3:  21  21  11  10

 From /proc/meminfo
    MemTotal:       791238320 kB
    HugePages_Total:        0
    Hugepagesize:        2048 kB

 From /etc/*release* /etc/*version*
    SuSE-release:
       SUSE Linux Enterprise Server 12 (x86_64)
       VERSION = 12
       PATCHLEVEL = 3
       # This file is deprecated and will be removed in a future service pack or release.
       # Please check /etc/os-release for details about this release.
    os-release:
       NAME="SLES"
       VERSION="12-SP3"
       VERSION_ID="12.3"
       PRETTY_NAME="SUSE Linux Enterprise Server 12 SP3"
       ID="sles"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:12:sp3"

 uname -a:
    Linux linux-4dlf 4.4.120-94.17-default #1 SMP Wed Mar 14 17:23:00 UTC 2018 (cf3a7bb)
    x86_64 x86_64 x86_64 GNU/Linux

 Kernel self-reported vulnerability status:

 CVE-2017-5754 (Meltdown):          Mitigation: PTI
 CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
 CVE-2017-5715 (Spectre variant 2): Mitigation: IBRS+IBPB

 run-level 3 Jan 26 03:15

 SPEC is set to: /home/cpu2017
    Filesystem      Type  Size  Used Avail Use% Mounted on
    /dev/sdb2       xfs   220G   35G  186G  16% /

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
```

(Continued on next page)

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6128
3.40 GHz)

SPECrate2017_int_base = 83.9

SPECrate2017_int_peak = 88.5

Platform Notes (Continued)

```
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   BIOS Cisco Systems, Inc. C220M5.4.0.1.139.1003182107 10/03/2018
   Memory:
    7x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
    17x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
 CC   500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
      525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CC   500.perlbench_r(peak) 502.gcc_r(peak)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CXXC 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base)
      541.leela_r(base)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 CXXC 520.omnetpp_r(peak) 523.xalancbmk_r(peak) 531.deepsjeng_r(peak)
      541.leela_r(peak)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------


==============================================================================
 FC   548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation.  All rights reserved.
```

(Continued on next page)

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Tested by: Cisco Systems

Test Date: Jan-2019
Hardware Availability: Aug-2017
Software Availability: Nov-2018

Compiler Version Notes (Continued)

```
--------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
```
icc -m64 -std=c11
```

C++ benchmarks:
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

Base Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-DSPEC_LP64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-DSPEC_LP64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

C++ benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Fortran benchmarks:
```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6128 3.40 GHz)

SPECrate2017_int_base =   83.9

SPECrate2017_int_peak =   88.5

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m64 -std=c11
```

502.gcc_r: `icc -m32 -std=c11 -L/opt/intel/lib/ia32`

C++ benchmarks (except as noted below):
```
icpc -m64
```

523.xalancbmk_r: `icpc -m32 -L/opt/intel/lib/ia32`

Fortran benchmarks:
```
ifort -m64
```

Peak Portability Flags

500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`

Peak Optimization Flags

C benchmarks:

500.perlbench_r: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -fno-strict-overflow -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

502.gcc_r: `-Wl,-z,muldefs -prof-gen`(pass 1) `-prof-use`(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-32/ -ljemalloc`

505.mcf_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

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Peak Optimization Flags (Continued)

525.x264_r: `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -fno-alias -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

557.xz_r: `Same as 505.mcf_r`

C++ benchmarks:

520.omnetpp_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

523.xalancbmk_r: `-Wl,-z,muldefs` -prof-gen(pass 1) -prof-use(pass 2) `-ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-32/ -ljemalloc`

531.deepsjeng_r: `Same as 520.omnetpp_r`

541.leela_r: `Same as 520.omnetpp_r`

Fortran benchmarks:
`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html

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You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

---

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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