



# SPEC CPU®2017 Integer Speed Result

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## Cisco Systems

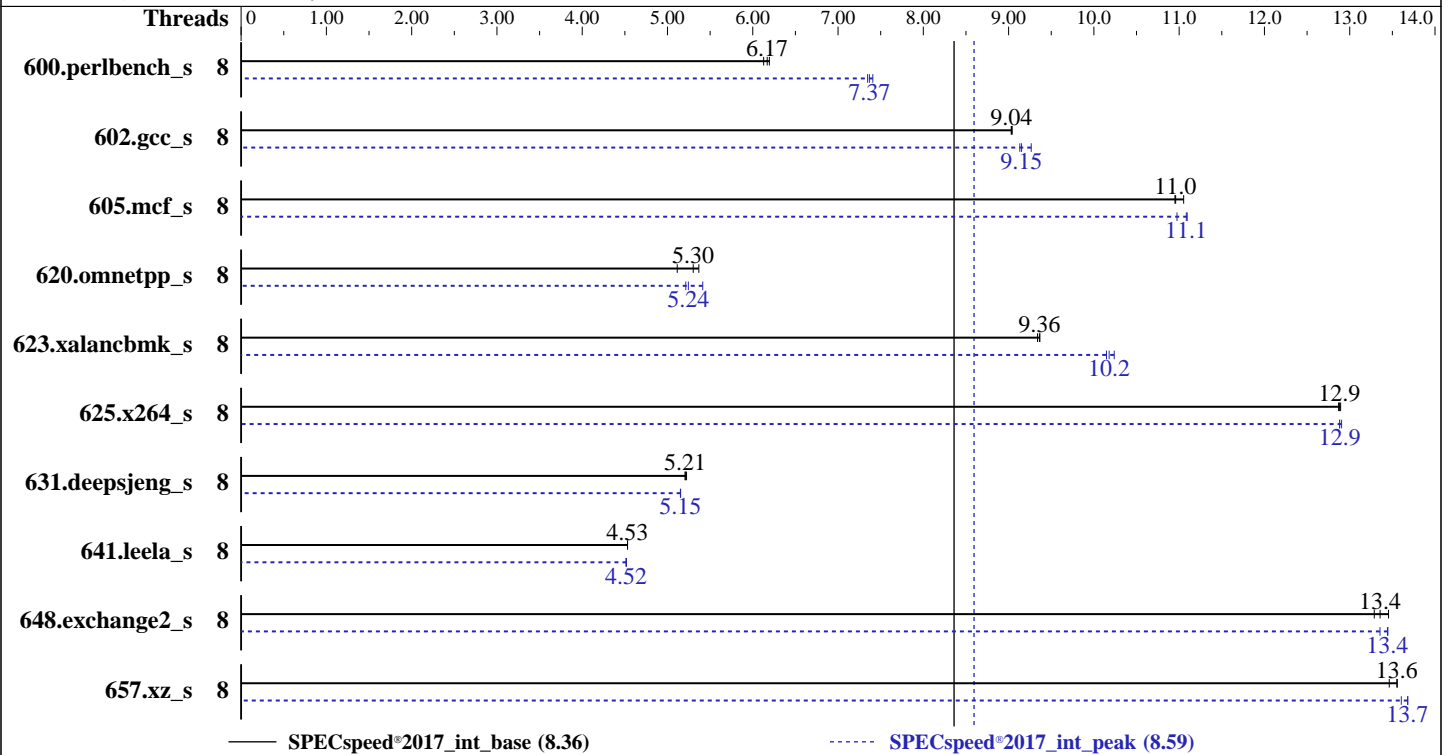
Cisco UCS C240 M5 (Intel Xeon Gold 5122  
3.60 GHz)

SPECspeed®2017\_int\_base = 8.36

SPECspeed®2017\_int\_peak = 8.59

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Dec-2018  
Hardware Availability: Aug-2017  
Software Availability: Oct-2018



### Hardware

CPU Name: Intel Xeon Gold 5122  
Max MHz: 3700  
Nominal: 3600  
Enabled: 8 cores, 2 chips  
Orderable: 1,2 Chips  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 16.5 MB I+D on chip per chip  
Other: None  
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)  
Storage: 1 x 600G SAS 10K RPM  
Other: None

### Software

OS: SUSE Linux Enterprise Server 12 SP2 (x86\_64)  
4.4.120-92.70-default  
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++  
Compiler for Linux;  
Fortran: Version 19.0.1.144 of Intel Fortran  
Compiler for Linux  
Parallel: Yes  
Firmware: Version 4.0.1 released Oct-2018  
File System: xfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 32/64-bit  
Other: jemalloc memory allocator V5.0.1  
Power Management: --



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## Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
600.perlbench_s	8	290	6.13	<b>288</b>	<b>6.17</b>	287	6.19	8	240	7.41	242	7.35	<b>241</b>	<b>7.37</b>
602.gcc_s	8	440	9.04	<b>441</b>	<b>9.04</b>	441	9.03	8	436	9.13	<b>435</b>	<b>9.15</b>	430	9.27
605.mcf_s	8	431	11.0	427	11.1	<b>431</b>	<b>11.0</b>	8	426	11.1	430	11.0	<b>426</b>	<b>11.1</b>
620.omnetpp_s	8	304	5.37	<b>308</b>	<b>5.30</b>	319	5.11	8	301	5.41	<b>311</b>	<b>5.24</b>	313	5.21
623.xalancbmk_s	8	152	9.34	151	9.37	<b>151</b>	<b>9.36</b>	8	138	10.2	140	10.1	<b>139</b>	<b>10.2</b>
625.x264_s	8	137	12.9	137	12.9	<b>137</b>	<b>12.9</b>	8	137	12.9	137	12.9	<b>137</b>	<b>12.9</b>
631.deepsjeng_s	8	<b>275</b>	<b>5.21</b>	274	5.22	275	5.21	8	278	5.15	<b>278</b>	<b>5.15</b>	278	5.15
641.leela_s	8	377	4.53	376	4.53	<b>377</b>	<b>4.53</b>	8	378	4.51	<b>378</b>	<b>4.52</b>	378	4.52
648.exchange2_s	8	221	13.3	<b>220</b>	<b>13.4</b>	219	13.5	8	220	13.4	219	13.4	<b>219</b>	<b>13.4</b>
657.xz_s	8	456	13.6	459	13.5	<b>456</b>	<b>13.6</b>	8	454	13.6	<b>452</b>	<b>13.7</b>	452	13.7

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## General Notes

Environment variables set by runcpu before the start of the run:

KMP\_AFFINITY = "granularity=fine,scatter"

LD\_LIBRARY\_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

OMP\_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM

memory using Redhat Enterprise Linux 7.4

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

sources available from jemalloc.net or <https://github.com/jemalloc/jemalloc/releases>



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### Platform Notes

#### BIOS Settings:

Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise  
Power Performance Tuning set to OS Controls  
SNC set to Disabled  
Patrol Scrub set to Disabled  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f  
running on linux-dkz7 Mon Dec 10 00:51:12 2018

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
<https://www.spec.org/cpu2017/Docs/config.html#sysinfo>

#### From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
 2 "physical id"s (chips)
 8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 0 5 9 13
physical 1: cores 3 4 6 7
```

#### From lscpu:

```
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 8
On-line CPU(s) list: 0-7
Thread(s) per core: 1
Core(s) per socket: 4
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
Stepping: 4
CPU MHz: 3499.349
CPU max MHz: 3700.0000
CPU min MHz: 1200.0000
BogoMIPS: 7183.11
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
```

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### Platform Notes (Continued)

```

L2 cache:                1024K
L3 cache:                16896K
NUMA node0 CPU(s):      0-3
NUMA node1 CPU(s):      4-7
Flags:                    fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmpperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtpr pdcm pcid sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx fl16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp_pkg_req intel_pt rsb_ctxsw spec_ctrl stibp
retpoline kaiser tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 cqm_llc cqm_occup_llc

```

```

/proc/cpuinfo cache data
cache size : 16896 KB

```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```

available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3
node 0 size: 385626 MB
node 0 free: 385195 MB
node 1 cpus: 4 5 6 7
node 1 size: 387054 MB
node 1 free: 386602 MB
node distances:
node  0  1
  0:  10  21
  1:  21  10

```

```

From /proc/meminfo
MemTotal:      791225660 kB
HugePages_Total:      0
Hugepagesize:    2048 kB

```

From /etc/\*release\* /etc/\*version\*

```

SuSE-release:
SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2
# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.
os-release:
NAME="SLES"
VERSION="12-SP2"

```

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### Platform Notes (Continued)

```
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="/o:suse:sles:12:sp2"
```

```
uname -a:
Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Dec 10 00:50
```

```
SPEC is set to: /home/cpu2017
Filesystem      Type  Size  Used Avail Use% Mounted on
/dev/sda2        xfs   500G  118G  383G  24% /
```

Additional information from dmidecode follows. **WARNING:** Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:  
12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666  
12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)

### Compiler Version Notes

```
=====  
C      | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base,  
      | peak) 625.x264_s(base, peak) 657.xz_s(base, peak)  
-----
```

```
icc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----
```

```
=====  
C++    | 620.omnetpp_s(base, peak) 623.xalanbmk_s(base, peak)  
      | 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)  
-----
```

```
icpc (ICC) 19.0.1.144 20181018  
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----  
=====
```

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## Compiler Version Notes (Continued)

Fortran | 648.exchange2\_s(base, peak)

-----  
ifort (IFORT) 19.0.1.144 20181018

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.  
-----

## Base Compiler Invocation

C benchmarks:

icc -m64 -std=c11

C++ benchmarks:

icpc -m64

Fortran benchmarks:

ifort -m64

## Base Portability Flags

600.perlbench\_s: -DSPEC\_LP64 -DSPEC\_LINUX\_X64

602.gcc\_s: -DSPEC\_LP64

605.mcf\_s: -DSPEC\_LP64

620.omnetpp\_s: -DSPEC\_LP64

623.xalancbmk\_s: -DSPEC\_LP64 -DSPEC\_LINUX

625.x264\_s: -DSPEC\_LP64

631.deepsjeng\_s: -DSPEC\_LP64

641.leela\_s: -DSPEC\_LP64

648.exchange2\_s: -DSPEC\_LP64

657.xz\_s: -DSPEC\_LP64

## Base Optimization Flags

C benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=3 -qopenmp -DSPEC\_OPENMP

-L/home/cpu2017/je5.0.1-64/ -ljemalloc

C++ benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div

-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc

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## Base Optimization Flags (Continued)

Fortran benchmarks:

```
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

## Peak Compiler Invocation

C benchmarks:

```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):

```
icpc -m64
```

```
623.xalancbmk_s: icpc -m32 -L/opt/intel/lib/ia32
```

Fortran benchmarks:

```
ifort -m64
```

## Peak Portability Flags

```
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64
```

## Peak Optimization Flags

C benchmarks:

```
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/home/cpu2017/je5.0.1-64/ -ljemalloc
```

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## Peak Optimization Flags (Continued)

602.gcc\_s: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2  
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3  
-no-prec-div -DSPEC\_SUPPRESS\_OPENMP -qopenmp  
-DSPEC\_OPENMP -L/home/cpu2017/je5.0.1-64/ -ljemalloc

605.mcf\_s: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

625.x264\_s: -w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

657.xz\_s: Same as 602.gcc\_s

C++ benchmarks:

620.omnetpp\_s: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

623.xalancbmk\_s: -w1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo  
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3  
-DSPEC\_SUPPRESS\_OPENMP -qopenmp -DSPEC\_OPENMP  
-L/home/cpu2017/je5.0.1-32/ -ljemalloc

631.deepsjeng\_s: Same as 620.omnetpp\_s

641.leela\_s: Same as 620.omnetpp\_s

Fortran benchmarks:

-w1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte  
-L/home/cpu2017/je5.0.1-64/ -ljemalloc

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.html>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.html>

You can also download the XML flags sources by saving the following links:

<http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml>

<http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml>





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Tested with SPEC CPU®2017 v1.0.2 on 2018-12-10 03:51:12-0500.  
Report generated on 2020-09-04 14:37:12 by CPU2017 PDF formatter v6255.  
Originally published on 2019-01-29.