SPEC® CINT2006 Result

Cisco Systems

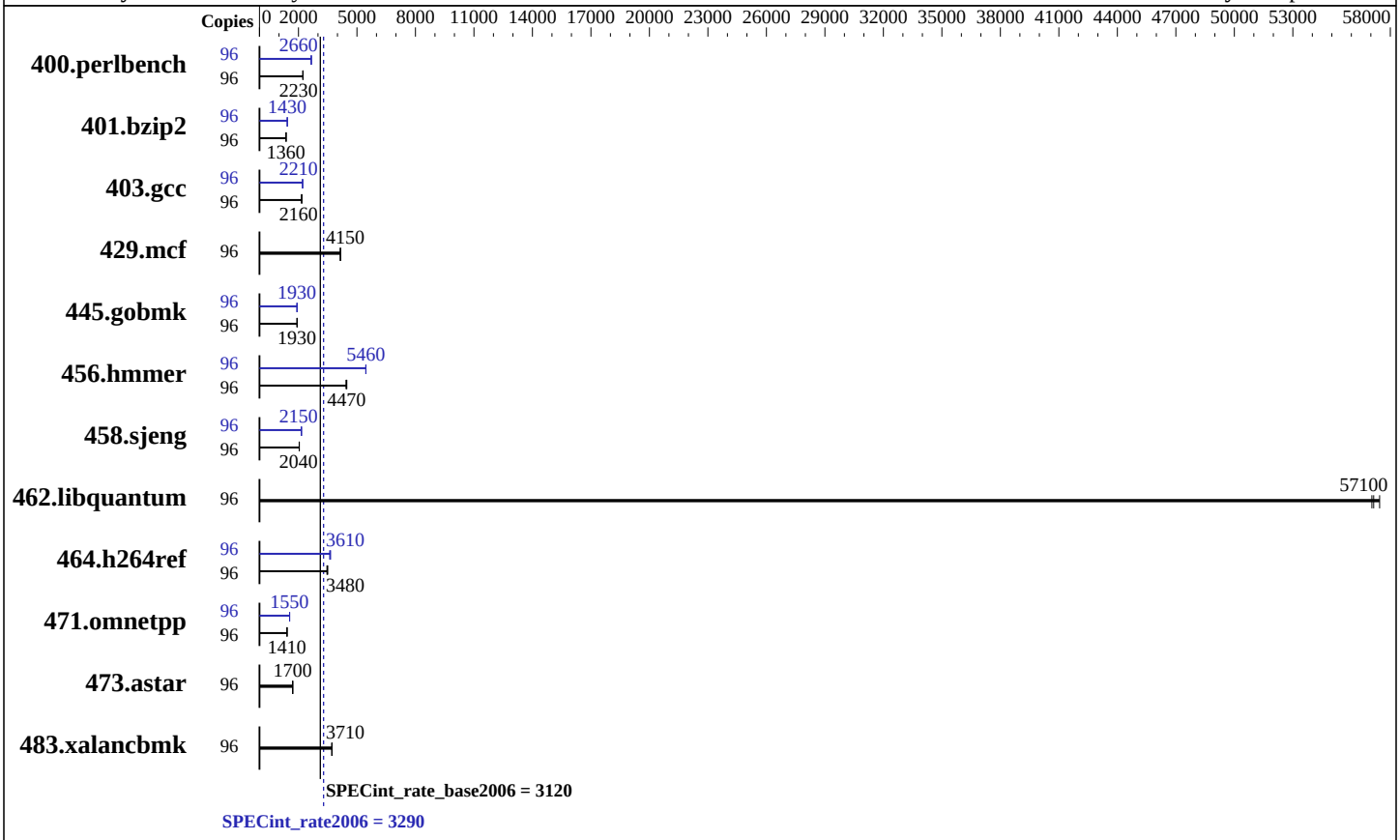
Cisco UCS B480 M5 (Intel Xeon Gold 6146, 3.20 GHz)

SPECint®_rate2006 = 3290

SPECint_rate_base2006 = 3120

CPU2006 license: 9019
Test sponsor: Cisco Systems
Tested by: Cisco Systems

Test date: Nov-2017
Hardware Availability: Aug-2017
Software Availability: Apr-2017



Hardware

CPU Name:	Intel Xeon Gold 6146
CPU Characteristics:	Intel Turbo Boost Technology up to 4.20 GHz
CPU MHz:	3200
FPU:	Integrated
CPU(s) enabled:	48 cores, 4 chips, 12 cores/chip, 2 threads/core
CPU(s) orderable:	2,4 chips
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	1 MB I+D on chip per core
L3 Cache:	24.75 MB I+D on chip per chip
Other Cache:	None
Memory:	768 GB (48 x 16 GB 2Rx4 PC4-2666V-R)
Disk Subsystem:	1 x 600 GB SAS HDD, 10K RPM
Other Hardware:	None

Software

Operating System:	SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.21-69-default
Compiler:	C/C++: Version 18.0.0.128 of Intel C/C++ Compiler for Linux; Fortran: Version 18.0.0.128 of Intel Fortran
Auto Parallel:	Yes
File System:	xfs
System State:	Run level 3 (multi-user)
Base Pointers:	32-bit
Peak Pointers:	32/64-bit
Other Software:	Microquill SmartHeap V10.2

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
400.perlbench	96	**421**	**2230**	422	2220	420	2230	96	352	2660	**353**	**2660**	354	2650
401.bzip2	96	678	1370	**680**	**1360**	680	1360	96	**650**	**1430**	648	1430	650	1420
403.gcc	96	356	2170	**357**	**2160**	358	2160	96	351	2200	**349**	**2210**	349	2220
429.mcf	96	211	4150	211	4150	**211**	**4150**	96	211	4150	211	4150	**211**	**4150**
445.gobmk	96	**521**	**1930**	521	1930	524	1920	96	522	1930	524	1920	**523**	**1930**
456.hmmer	96	202	4430	**200**	**4470**	200	4480	96	164	5450	164	5460	**164**	**5460**
458.sjeng	96	568	2040	**569**	**2040**	571	2040	96	539	2160	**540**	**2150**	541	2150
462.libquantum	96	34.6	57500	34.9	57100	**34.8**	**57100**	96	34.6	57500	34.9	57100	**34.8**	**57100**
464.h264ref	96	614	3460	607	3500	**611**	**3480**	96	582	3650	**588**	**3610**	589	3610
471.omnetpp	96	424	1420	425	1410	**425**	**1410**	96	**388**	**1550**	389	1540	388	1550
473.astar	96	**396**	**1700**	396	1700	395	1710	96	**396**	**1700**	396	1700	395	1710
483.xalancbmk	96	178	3710	**178**	**3710**	178	3720	96	178	3710	**178**	**3710**	178	3720

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
 Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6993
 Revision 6993 of 2015-11-06 (b5e8d4b4eb51ed28d7f98696cbe290c1)
 running on linux-vb5q Fri Nov 17 17:01:41 2017

 This section contains SUT (System Under Test) info as seen by
 some common utilities.  To remove or add to this section, see:
   http://www.spec.org/cpu2006/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 6146 CPU @ 3.20GHz
```

Continued on next page

Platform Notes (Continued)

```
        4 "physical id"s (chips)
        96 "processors"
     cores, siblings (Caution: counting these is hw and system dependent.  The
     following excerpts from /proc/cpuinfo might not be reliable.  Use with
     caution.)
        cpu cores : 12
        siblings  : 24
        physical 0: cores 0 3 4 5 6 7 16 18 19 20 21 22
        physical 1: cores 0 3 4 5 6 7 16 18 19 20 21 22
        physical 2: cores 0 1 3 9 10 16 18 19 24 25 26 27
        physical 3: cores 0 1 3 9 10 16 18 19 24 25 26 27
     cache size : 25344 KB

  From /proc/meminfo
     MemTotal:       791027864 kB
     HugePages_Total:       0
     Hugepagesize:       2048 kB

  From /etc/*release* /etc/*version*
     SuSE-release:
        SUSE Linux Enterprise Server 12 (x86_64)
        VERSION = 12
        PATCHLEVEL = 2
        # This file is deprecated and will be removed in a future service pack or
        release.
        # Please check /etc/os-release for details about this release.
     os-release:
        NAME="SLES"
        VERSION="12-SP2"
        VERSION_ID="12.2"
        PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
        ID="sles"
        ANSI_COLOR="0;32"
        CPE_NAME="cpe:/o:suse:sles:12:sp2"

  uname -a:
     Linux linux-vb5q 4.4.21-69-default #1 SMP Tue Oct 25 10:58:20 UTC 2016
     (9464f67) x86_64 x86_64 x86_64 GNU/Linux

  run-level 3 Jan 1 10:26

  SPEC is set to: /opt/cpu2006-1.2
     Filesystem     Type  Size  Used Avail Use% Mounted on
     /dev/sda1      xfs   280G   97G  183G  35% /
  Additional information from dmidecode:

     Warning: Use caution when you interpret this section. The 'dmidecode' program
     reads system data which is "intended to allow hardware to be accurately
     determined", but the intent may not be met, as there are frequent changes to
     hardware, firmware, and the "DMTF SMBIOS" standard.

    BIOS Cisco Systems, Inc. B480M5.3.2.2a.0.0919171641 09/19/2017
```

Continued on next page

Platform Notes (Continued)

```
      Memory:
       48x 0xCE00 M393A2G40EB2-CTD 16 GB 2 rank 2666 MHz

    (End of data from sysinfo program)
```

General Notes

```
 Environment variables set by runspec before the start of the run:
 LD_LIBRARY_PATH = "/opt/intel/lib/ia32:/opt/intel/lib/intel64:/opt/cpu2006-1.2/sh10.2"

  Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
  memory using Redhat Enterprise Linux 7.2
  Transparent Huge Pages enabled with:
  echo always > /sys/kernel/mm/transparent_hugepage/enabled
  Filesystem page cache cleared with:
  shell invocation of 'sync; echo 3 > /proc/sys/vm/drop_caches' prior to run
  runspec command invoked through numactl i.e.:
  numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:

```
icc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

C++ benchmarks:

```
icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Base Portability Flags

```
    400.perlbench: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX_IA32
        401.bzip2: -D_FILE_OFFSET_BITS=64
          403.gcc: -D_FILE_OFFSET_BITS=64
          429.mcf: -D_FILE_OFFSET_BITS=64
        445.gobmk: -D_FILE_OFFSET_BITS=64
        456.hmmer: -D_FILE_OFFSET_BITS=64
         458.sjeng: -D_FILE_OFFSET_BITS=64
    462.libquantum: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
      464.h264ref: -D_FILE_OFFSET_BITS=64
      471.omnetpp: -D_FILE_OFFSET_BITS=64
        473.astar: -D_FILE_OFFSET_BITS=64
    483.xalancbmk: -D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX
```

Base Optimization Flags

C benchmarks:
```
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
```

C++ benchmarks:
```
-xHOST -ipo -O3 -no-prec-div -qopt-prefetch -qopt-mem-layout-trans=3
-Wl,-z,muldefs -L/opt/cpu2006-1.2/sh10.2 -lsmartheap
```

Base Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

400.perlbench: `icc -m64`

401.bzip2: `icc -m64`

456.hmmer: `icc -m64`

458.sjeng: `icc -m64`

C++ benchmarks:
```
icpc -m32 -L/opt/intel/compilers_and_libraries_2018/linux/lib/ia32
```

Peak Portability Flags

400.perlbench: `-DSPEC_CPU_LP64 -DSPEC_CPU_LINUX_X64`
401.bzip2: `-DSPEC_CPU_LP64`
403.gcc: `-D_FILE_OFFSET_BITS=64`
429.mcf: `-D_FILE_OFFSET_BITS=64`
445.gobmk: `-D_FILE_OFFSET_BITS=64`
456.hmmer: `-DSPEC_CPU_LP64`
458.sjeng: `-DSPEC_CPU_LP64`
462.libquantum: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`
464.h264ref: `-D_FILE_OFFSET_BITS=64`
471.omnetpp: `-D_FILE_OFFSET_BITS=64`
473.astar: `-D_FILE_OFFSET_BITS=64`
483.xalancbmk: `-D_FILE_OFFSET_BITS=64 -DSPEC_CPU_LINUX`

Peak Optimization Flags

C benchmarks:

400.perlbench: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xHOST`(pass 2) `-par-num-threads=1`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-auto-ilp32 -qopt-mem-layout-trans=3`

401.bzip2: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xHOST`(pass 2) `-par-num-threads=1`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-qopt-prefetch -auto-ilp32 -qopt-mem-layout-trans=3`

403.gcc: `-xHOST -ipo -O3 -no-prec-div -qopt-mem-layout-trans=3`

429.mcf: `basepeak = yes`

445.gobmk: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xHOST`(pass 2) `-par-num-threads=1`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-qopt-mem-layout-trans=3`

456.hmmer: `-xHOST -ipo -O3 -no-prec-div -unroll2 -auto-ilp32 -qopt-mem-layout-trans=3`

458.sjeng: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xHOST`(pass 2) `-par-num-threads=1`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-unroll4 -auto-ilp32 -qopt-mem-layout-trans=3`

462.libquantum: `basepeak = yes`

464.h264ref: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xHOST`(pass 2) `-par-num-threads=1`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-unroll2 -qopt-mem-layout-trans=3`

C++ benchmarks:

471.omnetpp: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xHOST`(pass 2) `-par-num-threads=1`(pass 1) `-ipo`(pass 2) `-O3`(pass 2) `-no-prec-div`(pass 2) `-qopt-ra-region-strategy=block -qopt-mem-layout-trans=3 -Wl,-z,muldefs -L/opt/cpu2006-1.2/sh10.2 -lsmartheap`

473.astar: `basepeak = yes`

483.xalancbmk: `basepeak = yes`

Peak Other Flags

C benchmarks:

403.gcc: `-Dalloca=_alloca`

The flags files that were used to format this result can be browsed at
`http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.html`
`http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.html`

You can also download the XML flags sources by saving the following links:
`http://www.spec.org/cpu2006/flags/Intel-ic17.0-official-linux64-revF.xml`
`http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revH.xml`

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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