



SPEC[®] CFP2006 Result

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Cisco Systems

Cisco UCS B260 M4 (Intel Xeon E7-4809 v2, 1.90 GHz)

SPECfp[®]_rate2006 = **NC**

SPECfp_rate_base2006 = **NC**

CPU2006 license: 9019

Test sponsor: Cisco Systems

Tested by: Cisco Systems

Test date: Apr-2014

Hardware Availability: May-2014

Software Availability: Sep-2013

SPEC has determined that this result is not in compliance with the SPEC CPU2006 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a BIOS which included a version of the Intel MRC (Memory Reference Code) that is not supported by Cisco or Intel.

	Copies
410.bwaves	
416.gamess	
433.milc	
434.zeusmp	
435.gromacs	
436.cactusADM	
437.leslie3d	
444.namd	
447.dealII	
450.soplex	
453.povray	
454.calculix	
459.G	
465.tonto	
470.lbm	
481.wrf	
482.sphinx3	



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Hardware

CPU Name: Intel Xeon E7-4809 v2
 CPU Characteristics:
 CPU MHz: 1900
 FPU: Integrated
 CPU(s) enabled: 12 cores, 2 chips, 6 cores/chip, 2 threads/core
 CPU(s) orderable: 1,2 chip
 Primary Cache: 32 KB I + 32 KB D on chip per core
 Secondary Cache: 256 KB I+D on chip per core
 L3 Cache: 12 MB I+D on chip per chip
 Other Cache: None
 Memory: 256 GB (32 x 8 GB 2Rx4 PC3L-12800R-11, ECC, running at 1333 MHz and 11)
 Disk Subsystem: 1 X 300 GB 15000 RPM SAS
 Other Hardware: None

Software

Operating System: Red Hat Enterprise Linux Server release 6.4 (Santiago)
 Compiler: 2.6.32-358.el6.x86_64
 C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux;
 Fortran: Version 14.0.0.080 of Intel Fortran Studio XE for Linux
 Auto Parallel: No
 File System: ext4
 System State: Run level 3 (multi-user)
 Base Pointers: 32/64-bit
 Peak Pointers: 32/64-bit
 Other Software: None

Non-Compliant



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Results Table

Benchmark	Base								Peak							
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio		
410.bwaves	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
416.gamess	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
433.milc	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
434.zeusmp	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
435.gromacs	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
436.cactusADM	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
437.leslie3d	24	NC	NC	NC	NC	NC	NC	12	NC	NC	NC	NC	NC	NC		
444.namd	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
447.dealII	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
450.soplex	24	NC	NC	NC	NC	NC	NC	12	NC	NC	NC	NC	NC	NC		
453.povray	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
454.calculix	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
459.GemsFDTD	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
465.tonto	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
470.lbm	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
481.wrf	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		
482.sphinx3	24	NC	NC	NC	NC	NC	NC	24	NC	NC	NC	NC	NC	NC		

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"



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Platform Notes

```

Intel HT Technology = Enabled
CPU performance set to HPC
Power Technology set to Custom
CPU Power State C6 set to Disabled
CPU Power State C1 Enhanced set to Disabled
Memory RAS configuration set to Maximum Performance
DRAM Clock Throttling Set to Performance
Sysinfo program /opt/cpu2006-1.4/config/sysinfo.rev6818
$Rev: 6818 $ $Date:: 2012-07-17 # $ e86d1572650a6e4d596a3cee98f191
running on specompcpu Tue Apr 22 17:54:51 2014

```

This section contains SUT (System Under Test) info as seen by some common utilities. To remove or add to this section, see: <http://www.spec.org/cpu2006/config.html#sysinfo>

```

From /proc/cpuinfo
model name : Intel(R) Xeon(R) CPU E7-4809 v2 @ 1.90GHz
 2 "physical id" (chips)
 24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The
following excerpt from /proc/cpuinfo might not be reliable. Use with
caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5
cache size : 12288 KB

```

```

MemTotal:      264106280 kB
MmStgPages_Total:      0
Hugepagesize:   2048 kB

```

```

/usr/bin/lsb_release -d
Red Hat Enterprise Linux Server release 6.4 (Santiago)

```

```

From /etc/*release* /etc/*version*
redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

```

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Platform Notes (Continued)

```
uname -a:
Linux specompcpu 2.6.32-358.el6.x86_64 SMP #1 Jan 29 11:47:41 EST 2013
x86_64 x86_64 x86_64 GNU/Linux
```

```
run-level 3 Apr 21 14:37
```

```
SPEC is set to: /opt/cpu2006-1.4
Filesystem      Type      Size  Used Avail Use% Mounted on
/dev/sdal       ext4      275G  29G  232G  11% /
```

```
Additional information from dmidecode:
BIOS Cisco Systems, Inc. XM4-1.2.2.1.12.012920142034 01/29/2014
Memory:
32x 8 GB
32x 0xCE00 M393B1K70QB0-YK0 8 GB 1333 MHz 2 rank
16x NO DIMM NO DIMM
```

(End of data from smpinfo program)

General Notes

Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.4/libs/32:/opt/cpu2006-1.4/libs/64:/opt/cpu2006-1.4/sh"

```
Binaries compiled on a system with 1x Core i7-860 CPU + 8GB
memory using kernel EL 6.4
Transparent Huge Pages enabled with:
/sys/kernel/mm/redhat_transparent_hugepage/enabled
filesystem page cache cleared with:
echo 1 > /proc/sys/vm/drop_caches
runspec command invoked through numactl i.e.:
numactl --interleave=all runspec <etc>
```

Submitted_by: "Sheshgiri I (shei)" <shei@cisco.com>
Submitted: Mon May 5 14:01:08 EDT 2014
Submission: cpu2006-20140505-29480.sub

Submitted_by: "Sheshgiri I (shei)" <shei@cisco.com>
Submitted: Sat May 24 09:39:27 EDT 2014
Submission: cpu2006-20140505-29480.sub



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Base Compiler Invocation

C benchmarks:
icc -m64

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
icc -m64 ifort -m64

Base Portability Flags

410.bwaves: -DSPEC_CPU_LP64
416.gamess: -DSPEC_CPU_LP64
433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
450.soplex: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.blender: -DSPEC_CPU_LP64 -nofor_main
59.GemSFTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
482.splix3: -DSPEC_CPU_LP64

Base Optimization Flags

C benchmarks:
-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

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Base Optimization Flags (Continued)

C++ benchmarks:

-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Fortran benchmarks:

-xAVX -ipo -O3 -no-prec-div -opt-prefetch

Benchmarks using both Fortran and C:

-xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
-opt-mem-layout-trans=3

Peak Compiler Invocation

C benchmarks (except as noted below):

icc -m64

482.sphinx3: icc -m32

C++ benchmarks (except as noted below):

icc -m64

450.soplex: icc -m32

Fortran benchmarks:

ifort -m64

Benchmarks using both Fortran and C:

icc -m64 ifort -m64

Peak Portability Flags

410.bwaves: -DSPEC_CPU_LP64

416.gamess: -DSPEC_CPU_LP64

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Peak Portability Flags (Continued)

```

433.milc: -DSPEC_CPU_LP64
434.zeusmp: -DSPEC_CPU_LP64
435.gromacs: -DSPEC_CPU_LP64 -nofor_main
436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
437.leslie3d: -DSPEC_CPU_LP64
444.namd: -DSPEC_CPU_LP64
447.dealII: -DSPEC_CPU_LP64
453.povray: -DSPEC_CPU_LP64
454.calculix: -DSPEC_CPU_LP64 -nofor_main
459.GemsFDTD: -DSPEC_CPU_LP64
465.tonto: -DSPEC_CPU_LP64
470.lbm: -DSPEC_CPU_LP64
481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX

```

Peak Optimization Flags

C benchmarks:

```

433.milc: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -auto-ilp32

```

470.lbm: basepeak = yes

```

482.sphinx3: -xAVX -ipo -O3 -no-prec-div -opt-mem-layout-trans=3
-unroll2

```

C++ benchmarks:

```

444.namd: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -fno-alias -auto-ilp32

```

447.dealII: basepeak = yes

```

450.soplex: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -opt-malloc-options=3

```

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Peak Optimization Flags (Continued)

453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -unroll14 -ansi-align

Fortran benchmarks:

410.bwaves: basepeak = yes

416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -prof-use(pass 2) -unroll12
-inline-level1 -scalar-rep-

434.zeusmp: basepeak = yes

437.leslie3d: -xAVX -ipo -O3 -no-prec-div -opt-prefetch

459.GemsFDTD: basepeak = yes

465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -prof-use(pass 2) -unroll14 -auto
-inline-level1 -opt-malloc-options=3

Benchmarks using both Fortran and C:

455.gromacs: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
-no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
-prof-use(pass 2) -opt-prefetch -auto-ilp32

50.cactusADM: basepeak = yes

434.calculix: basepeak = yes

487.wrf: -xAVX -ipo -O3 -no-prec-div -auto-ilp32

The flags files that were used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html>

<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-revB.html>



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You can also download the XML flags sources by saving the following links

<http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml>
<http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2-20140128.xml>

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For other inquiries, please contact webmaster@spec.org.

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