SPEC® CFP2006 Result
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Cisco Systems

Cisco UCS C240 M3 (Intel Xeon E5-2650 v2, 2.60 GHz)

$SPECfp®_rate2006 = $ **558**

$SPECfp_rate_base2006 = $ 547
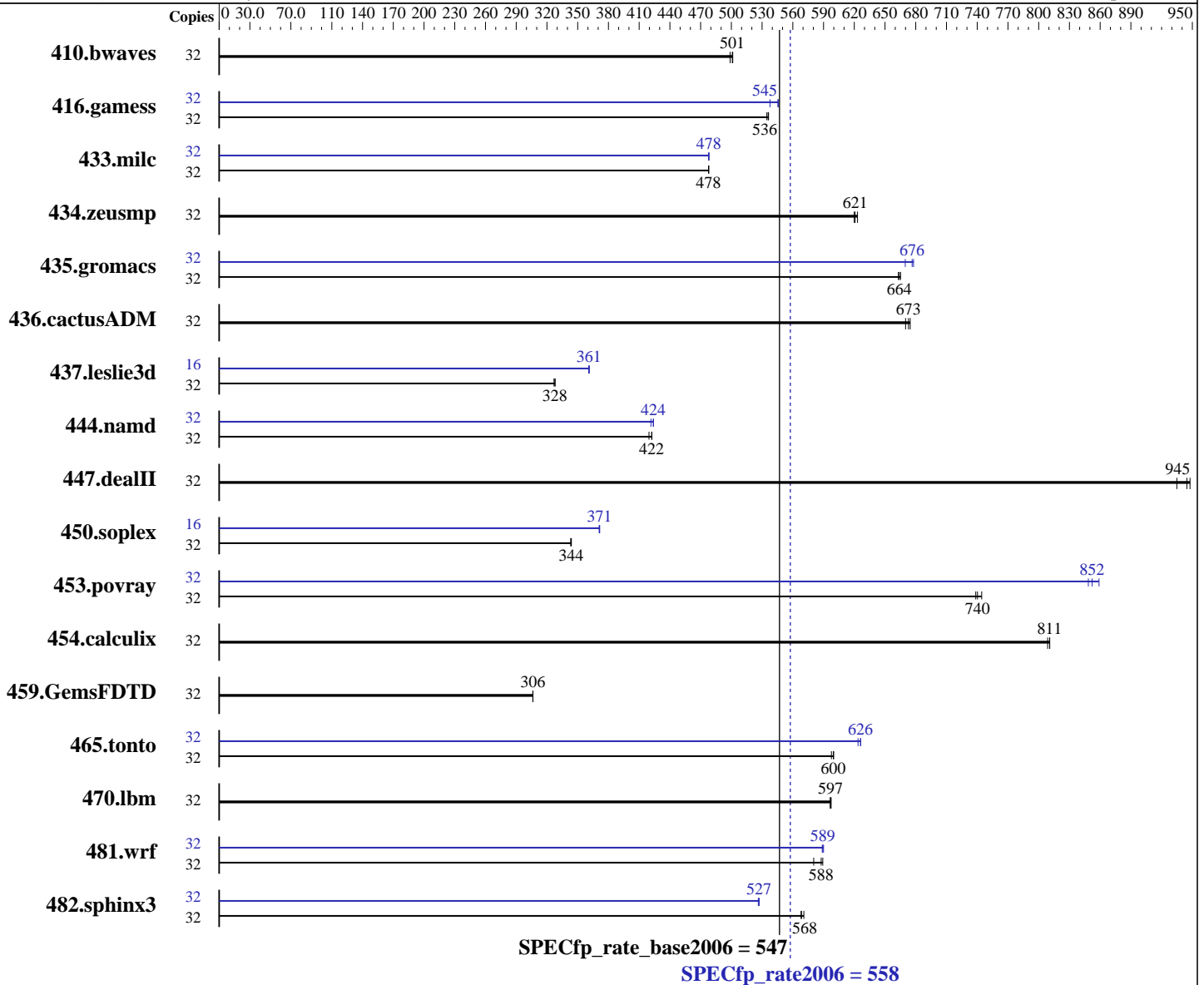
CPU2006 license: 9019	**Test date:** Oct-2013
Test sponsor: Cisco Systems	**Hardware Availability:** Sep-2013
Tested by: Cisco Systems	**Software Availability:** Sep-2013

Copies — graph scale: 0 30.0 70.0 110 140 170 200 230 260 290 320 350 380 410 440 470 500 530 560 590 620 650 680 710 740 770 800 830 860 890 950

- **410.bwaves** — 32 — 501
- **416.gamess** — 32 — 545 / 32 — 536
- **433.milc** — 32 — 478 / 32 — 478
- **434.zeusmp** — 32 — 621
- **435.gromacs** — 32 — 676 / 32 — 664
- **436.cactusADM** — 32 — 673
- **437.leslie3d** — 16 — 361 / 32 — 328
- **444.namd** — 32 — 424 / 32 — 422
- **447.dealII** — 32 — 945
- **450.soplex** — 16 — 371 / 32 — 344
- **453.povray** — 32 — 852 / 32 — 740
- **454.calculix** — 32 — 811
- **459.GemsFDTD** — 32 — 306
- **465.tonto** — 32 — 626 / 32 — 600
- **470.lbm** — 32 — 597
- **481.wrf** — 32 — 589 / 32 — 588
- **482.sphinx3** — 32 — 527 / 32 — 568

SPECfp_rate_base2006 = 547

SPECfp_rate2006 = 558

Hardware

CPU Name:	Intel Xeon E5-2650 v2
CPU Characteristics:	Intel Turbo Boost Technology up to 3.40 GHz
CPU MHz:	2600
FPU:	Integrated
CPU(s) enabled:	16 cores, 2 chips, 8 cores/chip, 2 threads/core
CPU(s) orderable:	1,2 chip
Primary Cache:	32 KB I + 32 KB D on chip per core
Secondary Cache:	256 KB I+D on chip per core

Continued on next page

Software

Operating System:	Red Hat Enterprise Linux Server release 6.4 (Santiago) 2.6.32-358.el6.x86_64
Compiler:	C/C++: Version 14.0.0.080 of Intel C++ Studio XE for Linux; Fortran: Version 14.0.0.080 of Intel Fortran Studio XE for Linux
Auto Parallel:	No
File System:	ext4

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L3 Cache:	20 MB I+D on chip per chip	System State:	Run level 3 (multi-user)
Other Cache:	None	Base Pointers:	32/64-bit
Memory:	128 GB (16 x 8 GB 2Rx4 PC3-14900R-13, ECC)	Peak Pointers:	32/64-bit
Disk Subsystem:	1 X 200 GB SSD	Other Software:	None
Other Hardware:	None		

Results Table

Benchmark	Base						Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
410.bwaves	32	**868**	**501**	867	501	872	499	32	**868**	**501**	867	501	872	499
416.gamess	32	**1169**	**536**	1172	535	1168	536	32	**1149**	**545**	1148	546	1165	538
433.milc	32	615	478	615	478	**615**	**478**	32	**615**	**478**	614	478	615	478
434.zeusmp	32	**469**	**621**	470	620	467	623	32	**469**	**621**	470	620	467	623
435.gromacs	32	**344**	**664**	345	663	343	665	32	341	670	**338**	**676**	337	678
436.cactusADM	32	571	670	567	675	**568**	**673**	32	571	670	567	675	**568**	**673**
437.leslie3d	32	917	328	920	327	**918**	**328**	16	417	361	416	361	**417**	**361**
444.namd	32	608	422	**608**	**422**	612	420	32	609	422	**606**	**424**	605	424
447.dealII	32	**388**	**945**	386	948	392	935	32	**388**	**945**	386	948	392	935
450.soplex	32	776	344	**777**	**344**	778	343	16	360	371	**359**	**371**	359	372
453.povray	32	**230**	**740**	231	739	229	744	32	**200**	**852**	201	848	198	859
454.calculix	32	326	809	**326**	**811**	326	811	32	326	809	**326**	**811**	326	811
459.GemsFDTD	32	**1108**	**306**	1108	306	1109	306	32	**1108**	**306**	1108	306	1109	306
465.tonto	32	525	600	**525**	**600**	527	598	32	**503**	**626**	505	624	503	626
470.lbm	32	736	597	737	597	**737**	**597**	32	736	597	737	597	**737**	**597**
481.wrf	32	**608**	**588**	607	589	616	580	32	607	589	**607**	**589**	606	590
482.sphinx3	32	**1097**	**568**	1093	571	1098	568	32	**1184**	**527**	1183	527	1185	526

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

    The numactl mechanism was used to bind copies to processors. The config file option 'submit'
    was used to generate numactl commands to bind each copy to a specific processor.
    For details, please see the config file.

Operating System Notes

    Stack size set to unlimited using "ulimit -s unlimited"

Platform Notes

    Intel HT Technology = Enabled
    CPU performance set to HPC
    Power Technology set to Custom

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Hardware Availability: Sep-2013

Software Availability: Sep-2013

Platform Notes (Continued)

```
  CPU Power State C6 set to Enabled
  CPU Power State C1 Enhanced set to Disabled
  Energy Performance policy set to Performances
  DRAM Clock Throttling Set to Performance
  LV DDR Mode set to Performance-mode
  DRAM Refresh Rate Set to 1x
   Sysinfo program /opt/cpu2006-1.2/config/sysinfo.rev6818
   $Rev: 6818 $ $Date:: 2012-07-17 #$ e86d102572650a6e4d596a3cee98f191
   running on localhost.localdomain Wed Oct 16 18:01:42 2013

   This section contains SUT (System Under Test) info as seen by
   some common utilities.  To remove or add to this section, see:
     http://www.spec.org/cpu2006/Docs/config.html#sysinfo

   From /proc/cpuinfo
      model name : Intel(R) Xeon(R) CPU E5-2650 v2 @ 2.60GHz
         2 "physical id"s (chips)
         32 "processors"
      cores, siblings (Caution: counting these is hw and system dependent.  The
      following excerpts from /proc/cpuinfo might not be reliable.  Use with
      caution.)
         cpu cores : 8
         siblings  : 16
         physical 0: cores 0 1 2 3 4 5 6 7
         physical 1: cores 0 1 2 3 4 5 6 7
      cache size : 20480 KB

   From /proc/meminfo
      MemTotal:       132124328 kB
      HugePages_Total:        0
      Hugepagesize:        2048 kB

   /usr/bin/lsb_release -d
      Red Hat Enterprise Linux Server release 6.4 (Santiago)

   From /etc/*release* /etc/*version*
      redhat-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
      system-release: Red Hat Enterprise Linux Server release 6.4 (Santiago)
      system-release-cpe: cpe:/o:redhat:enterprise_linux:6server:ga:server

   uname -a:
      Linux localhost.localdomain 2.6.32-358.el6.x86_64 #1 SMP Tue Jan 29 11:47:41
      EST 2013 x86_64 x86_64 x86_64 GNU/Linux

   run-level 3 Oct 16 17:50

   SPEC is set to: /opt/cpu2006-1.2
      Filesystem     Type     Size  Used Avail Use% Mounted on
      /dev/sda1      ext4     182G  125G   48G  73% /

   Additional information from dmidecode:
    BIOS Cisco Systems, Inc. C240M3.1.5.2.27.071120132247 07/11/2013
```
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Platform Notes (Continued)

```
   Memory:
    16x 0xAD00 HMT31GR7EFR4C-RD 8 GB 1866 MHz 2 rank
    8x NO DIMM NO DIMM

  (End of data from sysinfo program)
```

General Notes

```
Environment variables set by runspec before the start of the run:
LD_LIBRARY_PATH = "/opt/cpu2006-1.2/libs/32:/opt/cpu2006-1.2/libs/64:/opt/cpu2006-1.2/sh"

 Binaries compiled on a system with 1x Core i7-860 CPU + 8GB
 memory using RedHat EL 6.4
 Transparent Huge Pages enabled with:
 echo always > /sys/kernel/mm/redhat_transparent_hugepage/enabled
 Filesystem page cache cleared with:
 echo 1>       /proc/sys/vm/drop_caches
 runspec command invoked through numactl i.e.:
 numactl --interleave=all runspec <etc>
```

Base Compiler Invocation

C benchmarks:
```
    icc   -m64
```

C++ benchmarks:
```
    icpc  -m64
```

Fortran benchmarks:
```
    ifort -m64
```

Benchmarks using both Fortran and C:
```
    icc   -m64 ifort -m64
```

Base Portability Flags

```
    410.bwaves: -DSPEC_CPU_LP64
    416.gamess: -DSPEC_CPU_LP64
      433.milc: -DSPEC_CPU_LP64
    434.zeusmp: -DSPEC_CPU_LP64
   435.gromacs: -DSPEC_CPU_LP64 -nofor_main
 436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
   437.leslie3d: -DSPEC_CPU_LP64
      444.namd: -DSPEC_CPU_LP64
     447.dealII: -DSPEC_CPU_LP64
     450.soplex: -DSPEC_CPU_LP64
```

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Base Portability Flags (Continued)

```
    453.povray: -DSPEC_CPU_LP64
   454.calculix: -DSPEC_CPU_LP64 -nofor_main
  459.GemsFDTD: -DSPEC_CPU_LP64
     465.tonto: -DSPEC_CPU_LP64
      470.lbm: -DSPEC_CPU_LP64
       481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
    482.sphinx3: -DSPEC_CPU_LP64
```

Base Optimization Flags

C benchmarks:
```
    -xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
    -opt-mem-layout-trans=3
```

C++ benchmarks:
```
    -xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
    -opt-mem-layout-trans=3
```

Fortran benchmarks:
```
    -xAVX -ipo -O3 -no-prec-div -opt-prefetch
```

Benchmarks using both Fortran and C:
```
    -xAVX -ipo -O3 -no-prec-div -opt-prefetch -auto-p32 -ansi-alias
    -opt-mem-layout-trans=3
```

Peak Compiler Invocation

C benchmarks (except as noted below):
```
    icc    -m64
```

```
    482.sphinx3: icc -m32
```

C++ benchmarks (except as noted below):
```
    icpc    -m64
```

```
     450.soplex: icpc -m32
```

Fortran benchmarks:
```
    ifort -m64
```

Benchmarks using both Fortran and C:
```
    icc    -m64 ifort -m64
```

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Peak Portability Flags

```
    410.bwaves: -DSPEC_CPU_LP64
   416.gamess: -DSPEC_CPU_LP64
      433.milc: -DSPEC_CPU_LP64
   434.zeusmp: -DSPEC_CPU_LP64
  435.gromacs: -DSPEC_CPU_LP64 -nofor_main
 436.cactusADM: -DSPEC_CPU_LP64 -nofor_main
   437.leslie3d: -DSPEC_CPU_LP64
      444.namd: -DSPEC_CPU_LP64
     447.dealII: -DSPEC_CPU_LP64
    453.povray: -DSPEC_CPU_LP64
   454.calculix: -DSPEC_CPU_LP64 -nofor_main
 459.GemsFDTD: -DSPEC_CPU_LP64
     465.tonto: -DSPEC_CPU_LP64
      470.lbm: -DSPEC_CPU_LP64
       481.wrf: -DSPEC_CPU_LP64 -DSPEC_CPU_CASE_FLAG -DSPEC_CPU_LINUX
```

Peak Optimization Flags

C benchmarks:

```
    433.milc: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -auto-ilp32

     470.lbm: basepeak = yes

  482.sphinx3: -xAVX -ipo -O3 -no-prec-div -opt-mem-layout-trans=3
          -unroll2
```

C++ benchmarks:

```
    444.namd: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -fno-alias -auto-ilp32

    447.dealII: basepeak = yes

   450.soplex: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -opt-malloc-options=3

   453.povray: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
          -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
          -prof-use(pass 2) -unroll4 -ansi-alias
```

Fortran benchmarks:

Continued on next page

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Peak Optimization Flags (Continued)

410.bwaves: basepeak = yes

416.gamess: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
            -no-prec-div(pass 2) -prof-use(pass 2) -unroll2
            -inline-level=0 -scalar-rep-

434.zeusmp: basepeak = yes

437.leslie3d: -xAVX -ipo -O3 -no-prec-div -opt-prefetch

459.GemsFDTD: basepeak = yes

465.tonto: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
           -no-prec-div(pass 2) -prof-use(pass 2) -unroll4 -auto
           -inline-calloc -opt-malloc-options=3

Benchmarks using both Fortran and C:

435.gromacs: -xAVX(pass 2) -prof-gen(pass 1) -ipo(pass 2) -O3(pass 2)
             -no-prec-div(pass 2) -opt-mem-layout-trans=3(pass 2)
             -prof-use(pass 2) -opt-prefetch -auto-ilp32

436.cactusADM: basepeak = yes

454.calculix: basepeak = yes

481.wrf: -xAVX -ipo -O3 -no-prec-div -auto-ilp32

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.html
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2006/flags/Intel-ic14.0-official-linux64.20140128.xml
http://www.spec.org/cpu2006/flags/Cisco-Platform-Settings-V1.2.20130717.xml

For questions about this result, please contact the tester.
For other inquiries, please contact webmaster@spec.org.

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