



# SPEC® CINT2006 Result

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## IBM Corporation

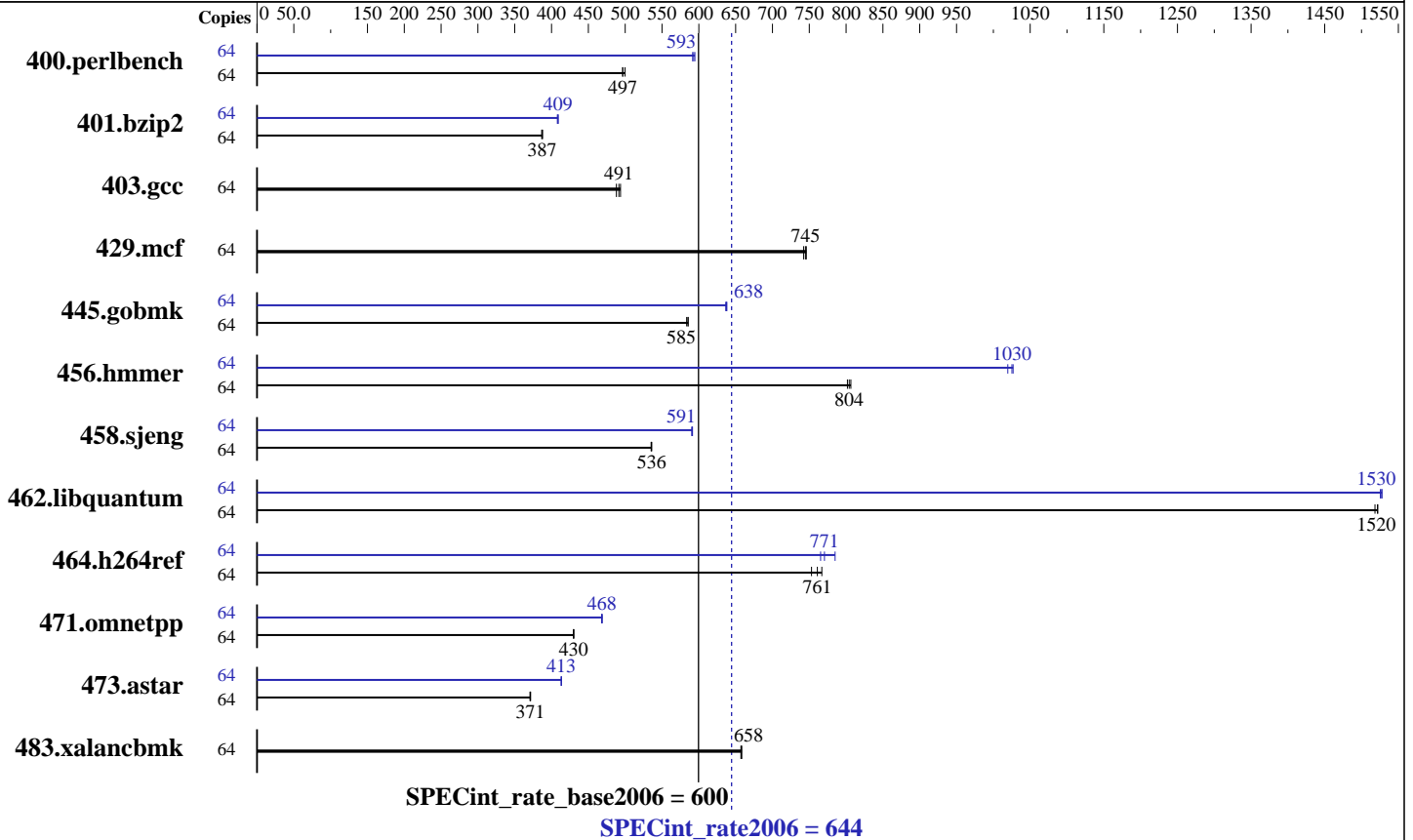
SPECint®\_rate2006 = 644

## IBM BladeCenter HX5 (Intel Xeon L7555)

SPECint\_rate\_base2006 = 600

CPU2006 license: 11  
Test sponsor: IBM Corporation  
Tested by: IBM Corporation

Test date: Apr-2010  
Hardware Availability: Jun-2010  
Software Availability: Jan-2010



### Hardware

CPU Name: Intel Xeon L7555  
 CPU Characteristics: Intel Turbo Boost Technology up to 2.53 GHz  
 CPU MHz: 1867  
 FPU: Integrated  
 CPU(s) enabled: 32 cores, 4 chips, 8 cores/chip, 2 threads/core  
 CPU(s) orderable: 1,2,3,4 chips  
 Primary Cache: 32 KB I + 32 KB D on chip per core  
 Secondary Cache: 256 KB I+D on chip per core  
 L3 Cache: 24 MB I+D on chip per chip  
 Other Cache: None  
 Memory: 256 GB (32 x 8 GB PC3-8500R, Quad Rank, running at 978 MHz)  
 Disk Subsystem: 2 x 50 GB SATA, SSD  
 Other Hardware: None

### Software

Operating System: SuSE Linux Enterprise Server 11 (x86\_64), Kernel 2.6.27.19-5-default  
 Compiler: Intel C++ Professional Compiler for IA32 and Intel 64, Version 11.1  
 Build 20091130 Package ID: l\_cproc\_p\_11.1.064  
 Auto Parallel: No  
 File System: ext3  
 System State: Run level 3 (multi-user)  
 Base Pointers: 32-bit  
 Peak Pointers: 32/64-bit  
 Other Software: Microquill SmartHeap V8.1  
 Binutils 2.18.50.0.7.20080502



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## Results Table

Benchmark	Base								Peak							
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio		
400.perlbench	64	1251	500	1259	497	<u>1259</u>	<u>497</u>	64	1052	595	<u>1054</u>	<u>593</u>	1057	592		
401.bzip2	64	1597	387	<u>1595</u>	<u>387</u>	1592	388	64	1514	408	1510	409	<u>1511</u>	<u>409</u>		
403.gcc	64	1056	488	<u>1048</u>	<u>491</u>	1044	494	64	1056	488	<u>1048</u>	<u>491</u>	1044	494		
429.mcf	64	782	746	786	742	<u>784</u>	<u>745</u>	64	782	746	786	742	<u>784</u>	<u>745</u>		
445.gobmk	64	1151	583	1147	586	<u>1147</u>	<u>585</u>	64	1052	638	<u>1053</u>	<u>638</u>	1055	637		
456.hammer	64	745	802	<u>742</u>	<u>804</u>	740	806	64	586	1020	<u>582</u>	<u>1030</u>	582	1030		
458.sjeng	64	<u>1445</u>	<u>536</u>	1445	536	1447	535	64	1309	591	<u>1310</u>	<u>591</u>	1312	590		
462.libquantum	64	<u>871</u>	<u>1520</u>	871	1520	873	1520	64	869	1530	868	1530	<u>868</u>	<u>1530</u>		
464.h264ref	64	1846	767	1881	753	<u>1861</u>	<u>761</u>	64	<u>1838</u>	<u>771</u>	1850	765	1804	785		
471.omnetpp	64	930	430	<u>930</u>	<u>430</u>	931	430	64	<u>854</u>	<u>468</u>	853	469	855	468		
473.astar	64	1209	372	1212	371	<u>1210</u>	<u>371</u>	64	<u>1087</u>	<u>413</u>	1087	413	1088	413		
483.xalancbmk	64	<u>671</u>	<u>658</u>	671	658	672	657	64	<u>671</u>	<u>658</u>	671	658	672	657		

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The config file option 'submit' was used.  
numactl was used to bind copies to the cores

## Platform Notes

Turbo Boost set to Traditional  
Demand Scrub disabled

## General Notes

'ulimit -s unlimited' was used to set the stack size to unlimited prior to run

## Base Compiler Invocation

C benchmarks:  
icc -m32

C++ benchmarks:  
icpc -m32



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## Base Portability Flags

400.perlbench: -DSPEC\_CPU\_LINUX\_IA32  
462.libquantum: -DSPEC\_CPU\_LINUX  
483.xalancbmk: -DSPEC\_CPU\_LINUX

## Base Optimization Flags

C benchmarks:  
-xSSE4.2 -ipo -O3 -no-prec-div -static -opt-prefetch

C++ benchmarks:  
-xSSE4.2 -ipo -O3 -no-prec-div -opt-prefetch -Wl,-z,muldefs  
-L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-32bit -lsmartheap

## Base Other Flags

C benchmarks:  
403.gcc: -Dalloca=\_alloca

## Peak Compiler Invocation

C benchmarks (except as noted below):  
icc -m32

401.bzip2: icc -m64

456.hmmer: icc -m64

458.sjeng: icc -m64

462.libquantum: icc -m64

C++ benchmarks (except as noted below):  
icpc -m32

473.astar: icpc -m64

## Peak Portability Flags

400.perlbench: -DSPEC\_CPU\_LINUX\_IA32  
401.bzip2: -DSPEC\_CPU\_LP64

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## Peak Portability Flags (Continued)

456.hmmcr: -DSPEC\_CPU\_LP64  
 458.sjeng: -DSPEC\_CPU\_LP64  
 462.libquantum: -DSPEC\_CPU\_LP64 -DSPEC\_CPU\_LINUX  
 473.astar: -DSPEC\_CPU\_LP64  
 483.xalancbmk: -DSPEC\_CPU\_LINUX

## Peak Optimization Flags

C benchmarks:

400.perlbench: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
 -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)  
 -prof-use(pass 2) -ansi-alias

401.bzip2: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
 -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)  
 -prof-use(pass 2) -opt-prefetch -ansi-alias -auto-ilp32

403.gcc: basepeak = yes

429.mcf: basepeak = yes

445.gobmk: -xSSE4.2(pass 2) -prof-gen(pass 1) -prof-use(pass 2) -O2  
 -ipo -no-prec-div -ansi-alias

456.hmmcr: -xSSE4.2 -ipo -O3 -no-prec-div -static -unroll2  
 -ansi-alias -auto-ilp32

458.sjeng: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
 -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)  
 -prof-use(pass 2) -unroll4 -auto-ilp32

462.libquantum: -xSSE4.2 -ipo -O3 -no-prec-div -static -auto-ilp32  
 -opt-prefetch

464.h264ref: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
 -O3(pass 2) -no-prec-div(pass 2) -static(pass 2)  
 -prof-use(pass 2) -unroll2 -ansi-alias

C++ benchmarks:

471.omnetpp: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)  
 -ansi-alias -opt-ra-region-strategy=block -Wl,-z,muldefs  
 -L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-32bit -lsmartheap

473.astar: -xSSE4.2(pass 2) -prof-gen(pass 1) -ipo(pass 2)  
 -O3(pass 2) -no-prec-div(pass 2) -prof-use(pass 2)  
 -ansi-alias -opt-ra-region-strategy=routine -Wl,-z,muldefs

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## Peak Optimization Flags (Continued)

473.astar (continued):

-L/home/cmplr/usr3/alrahate/cpu2006.1.1.ic11.1/libic11.1-64bit -lsmartheap64

483.xalancbmk: basepeak = yes

## Peak Other Flags

C benchmarks:

403.gcc: -Dalloca=\_alloca

The flags file that was used to format this result can be browsed at

<http://www.spec.org/cpu2006/flags/Intel-ic11.1-linux64-revE.20100330.03.html>

You can also download the XML flags source by saving the following link:

<http://www.spec.org/cpu2006/flags/Intel-ic11.1-linux64-revE.20100330.03.xml>

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For other inquiries, please contact [webmaster@spec.org](mailto:webmaster@spec.org).

Tested with SPEC CPU2006 v1.1.

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